

FIG. 1

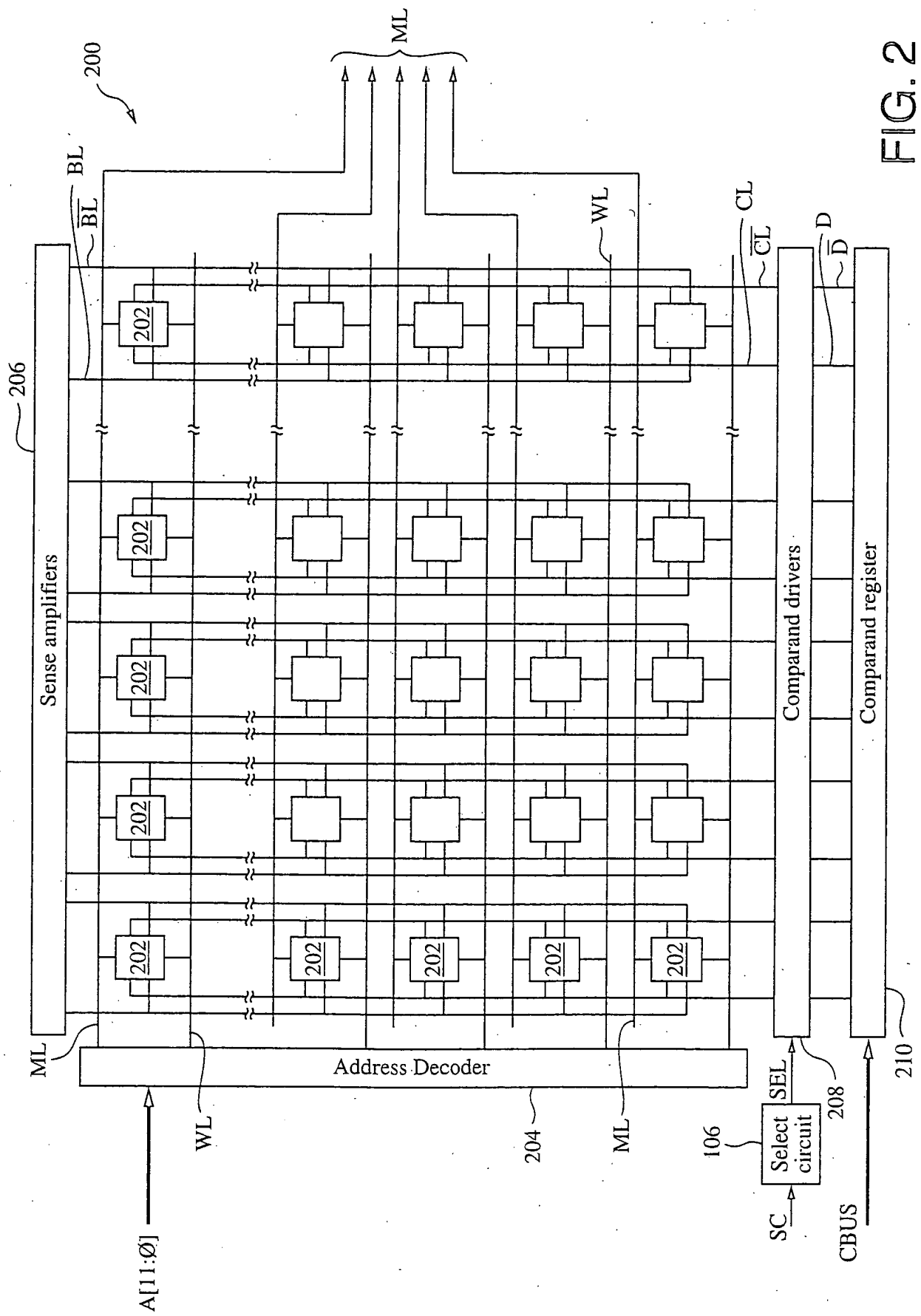


FIG. 2

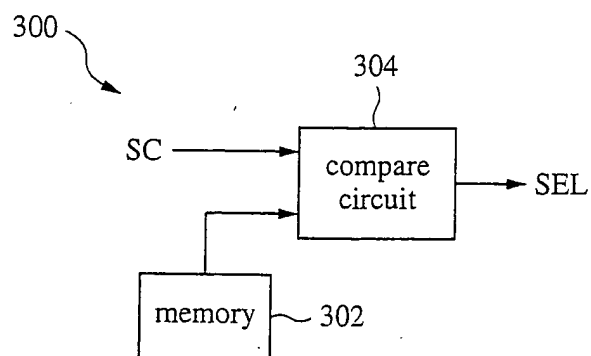


FIG. 3

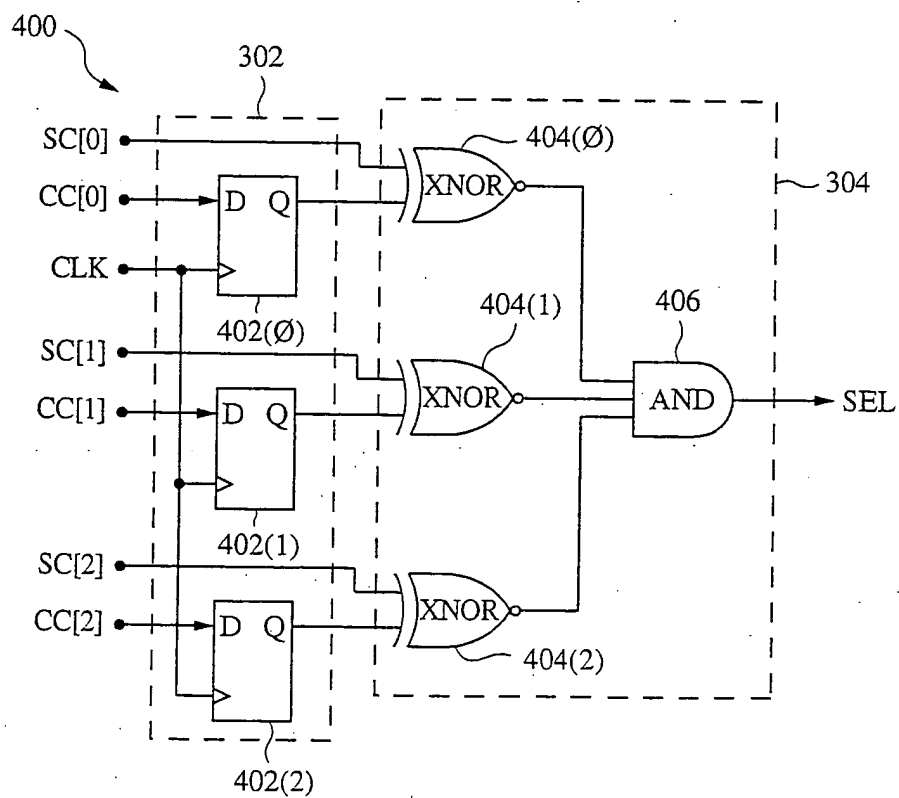


FIG. 4

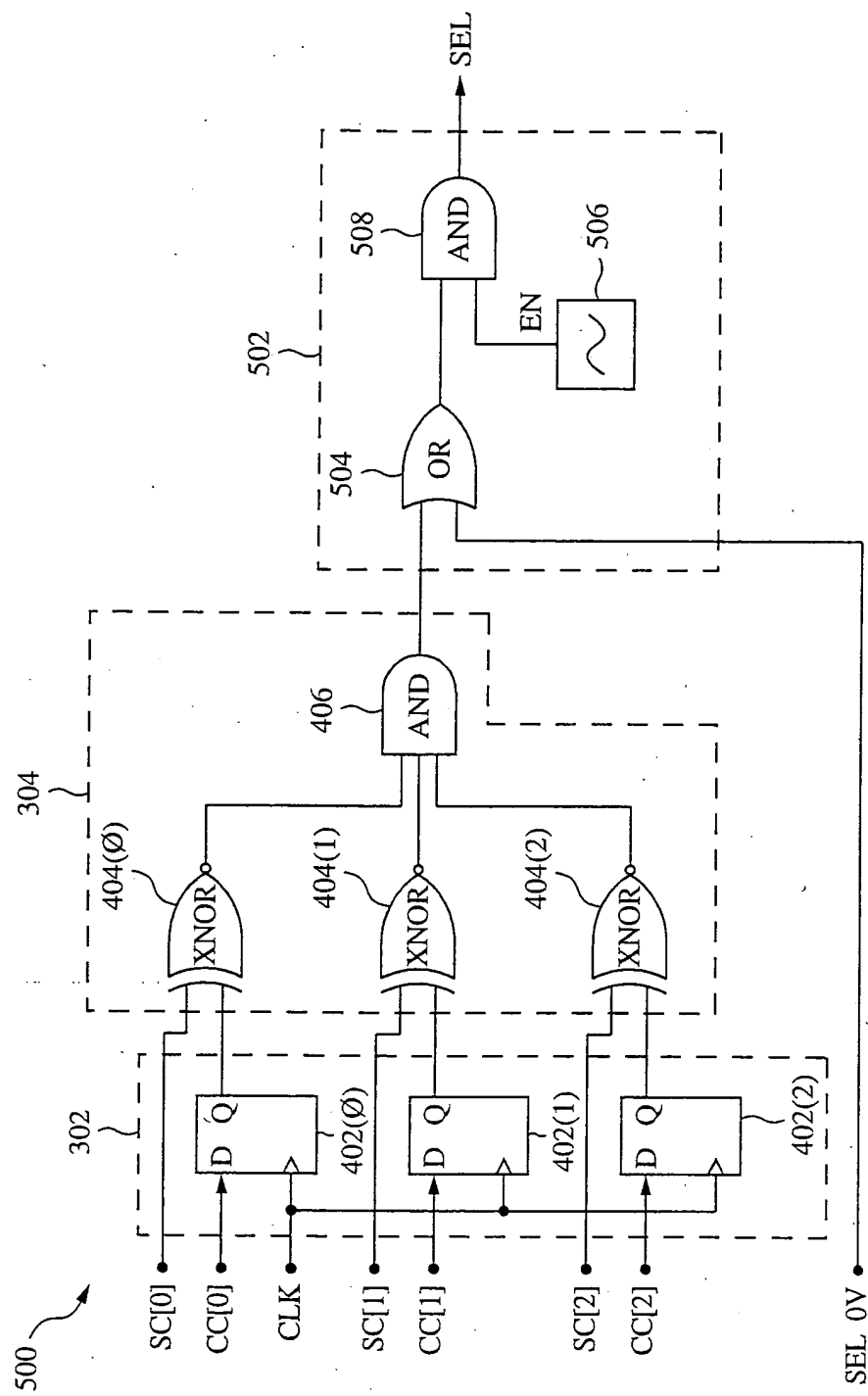


FIG. 5

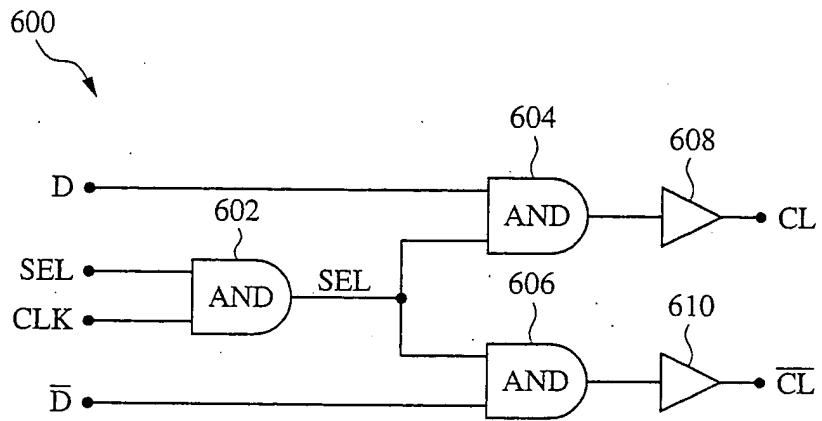


FIG. 6

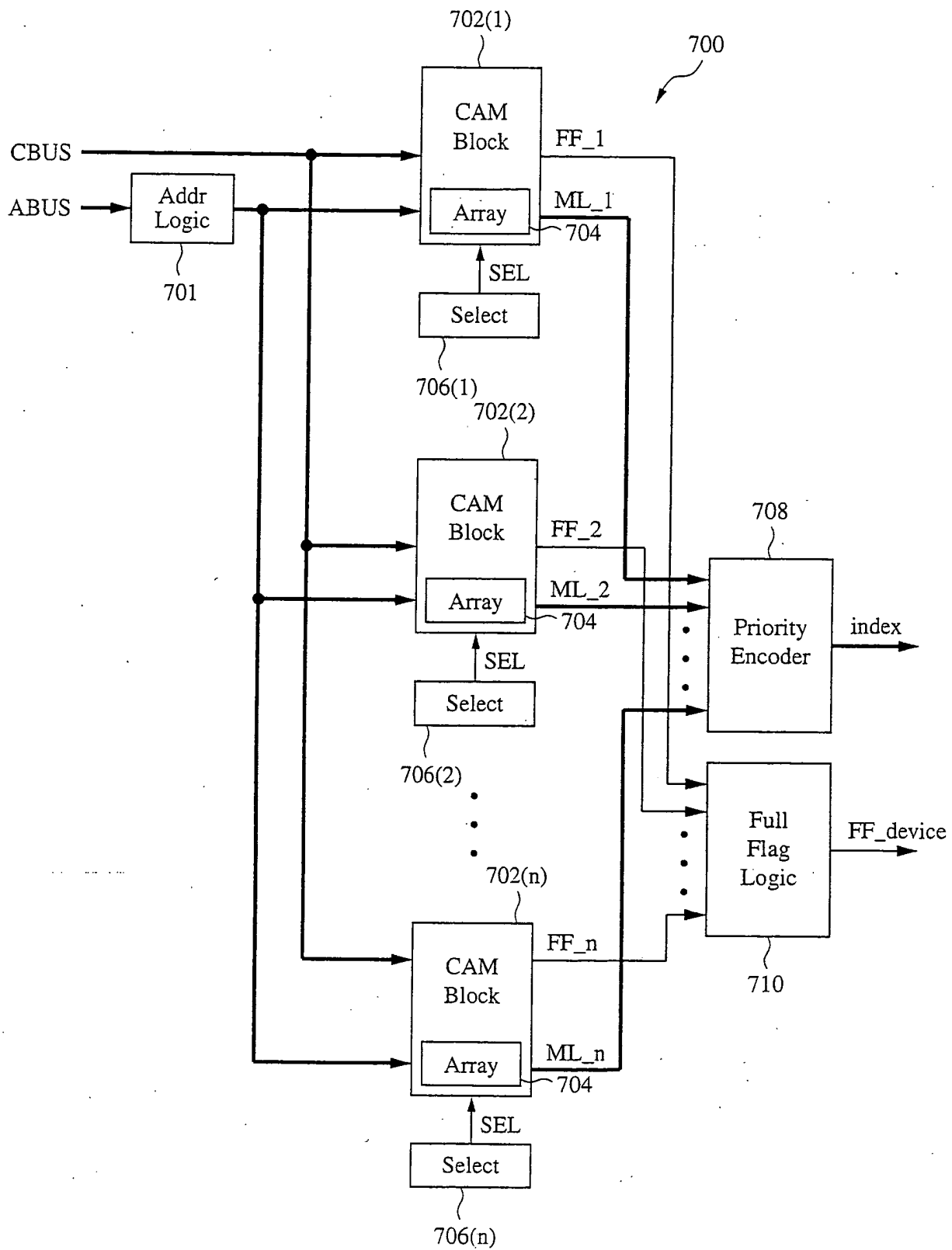


FIG. 7

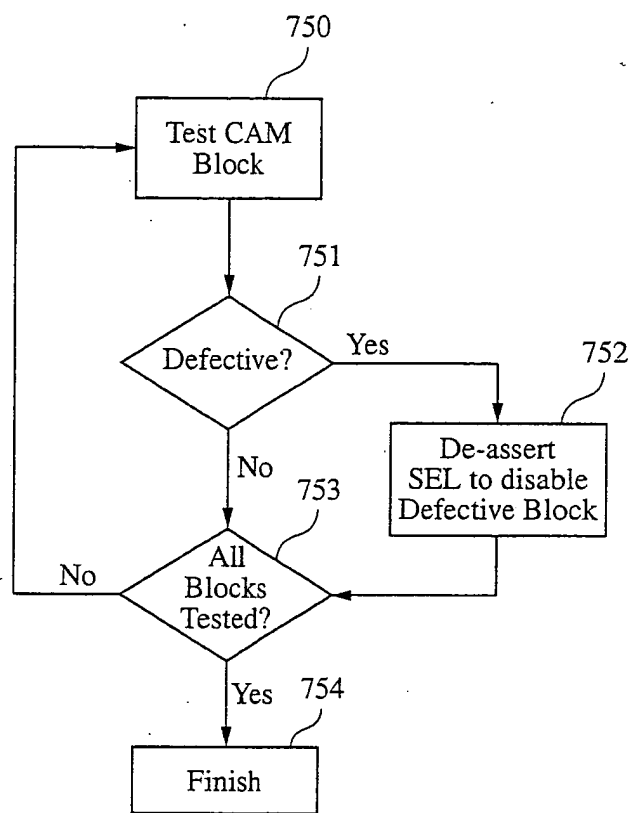


FIG. 8

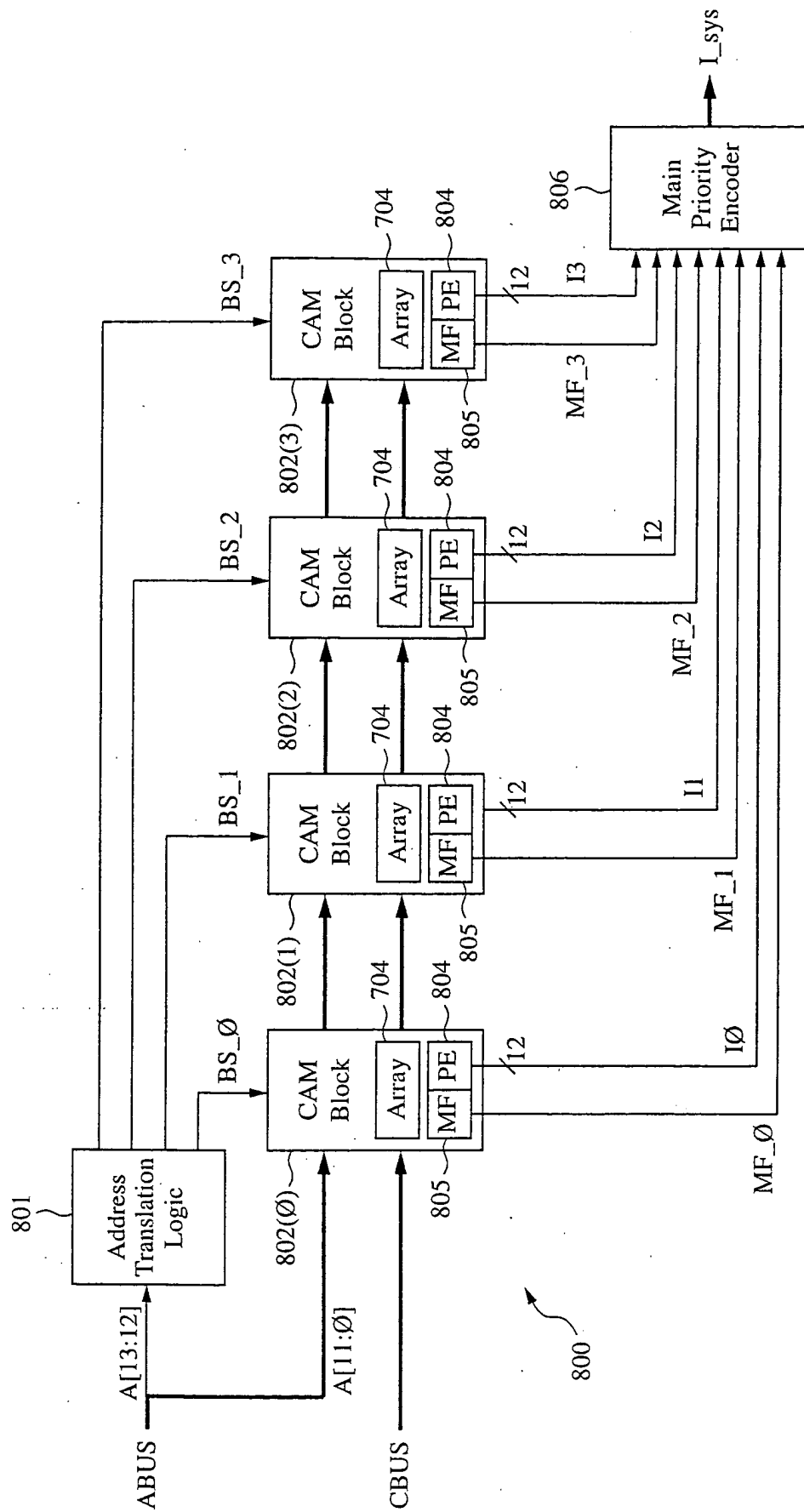


FIG. 9

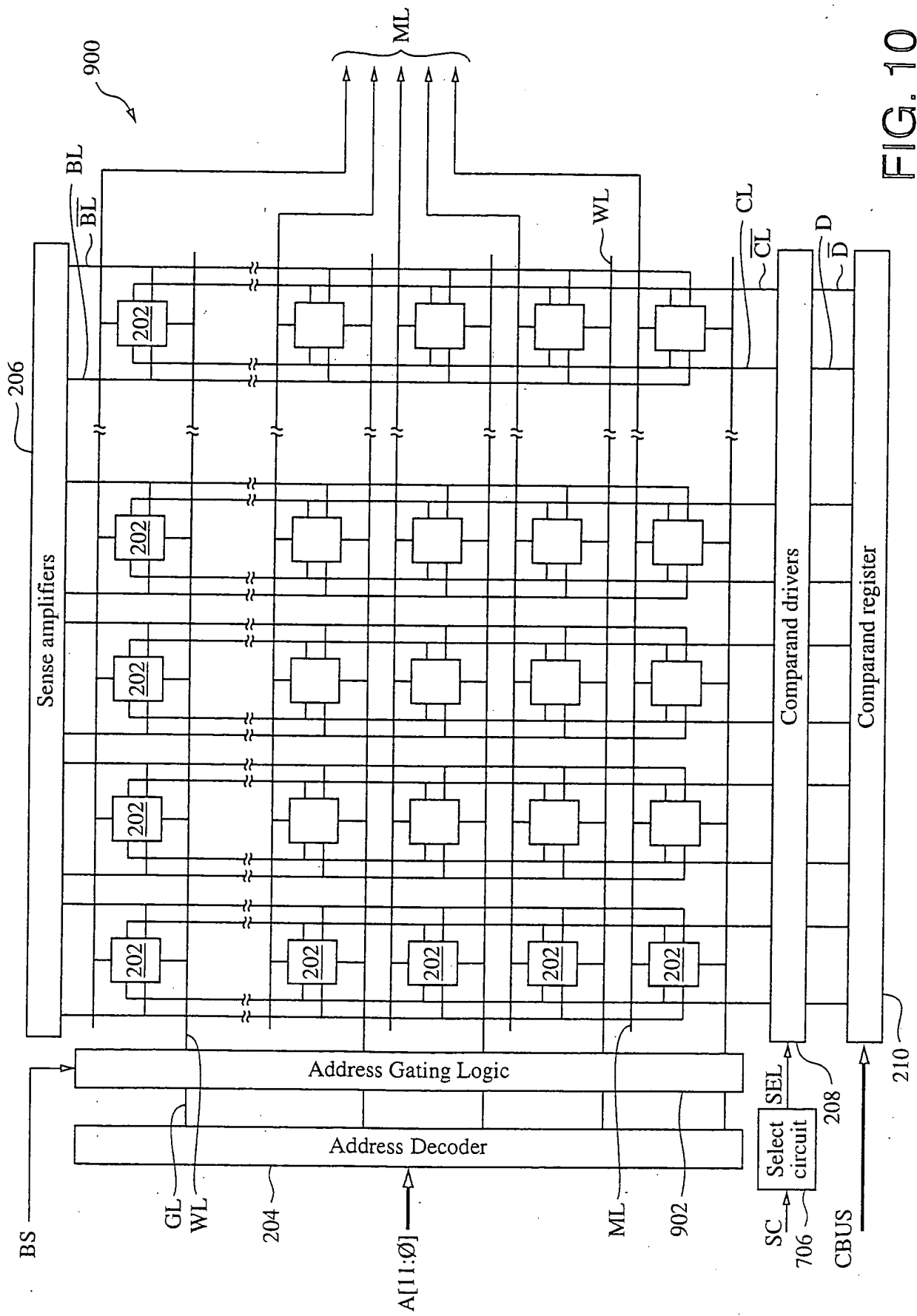


FIG. 10

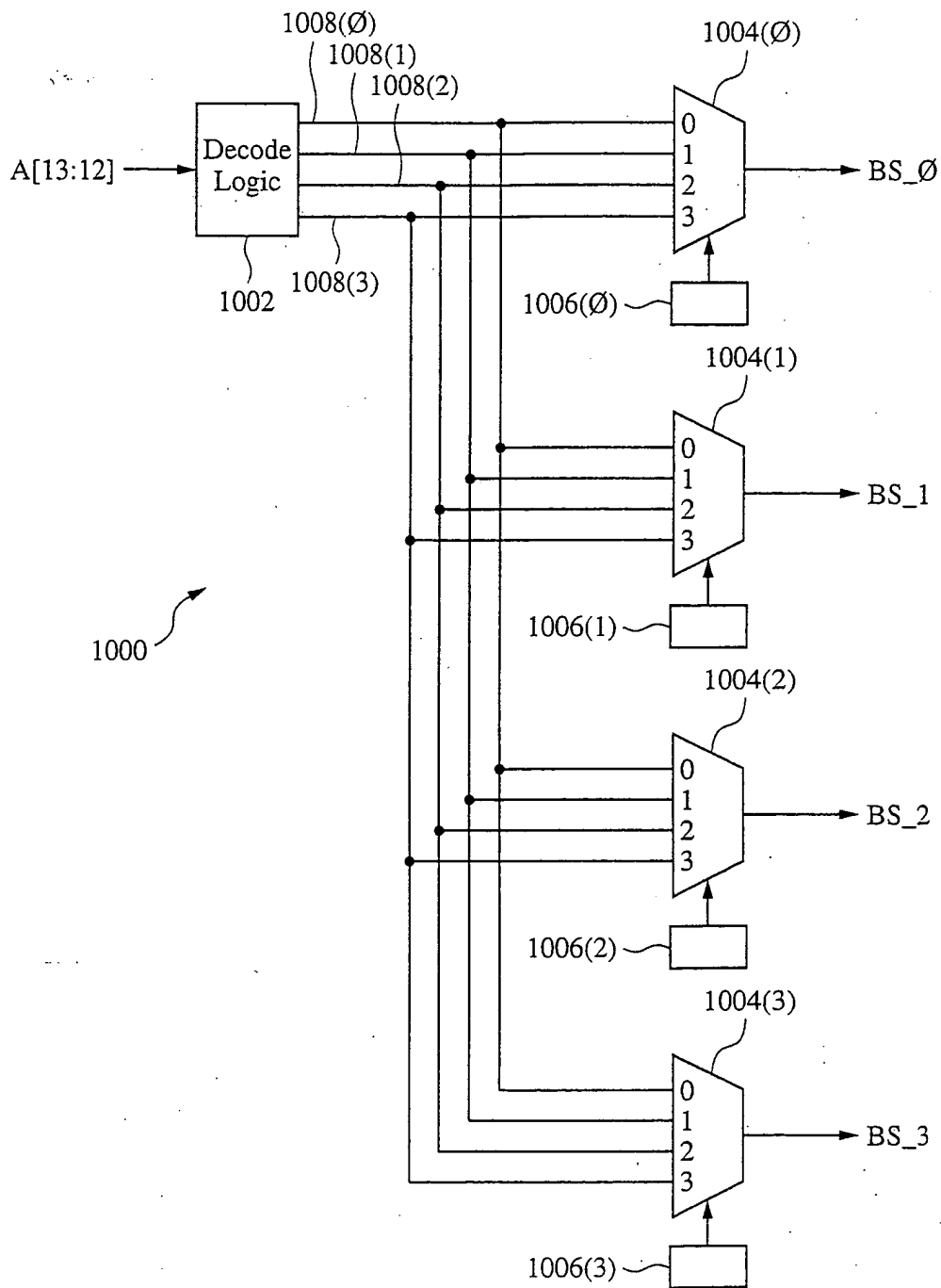


FIG. 11

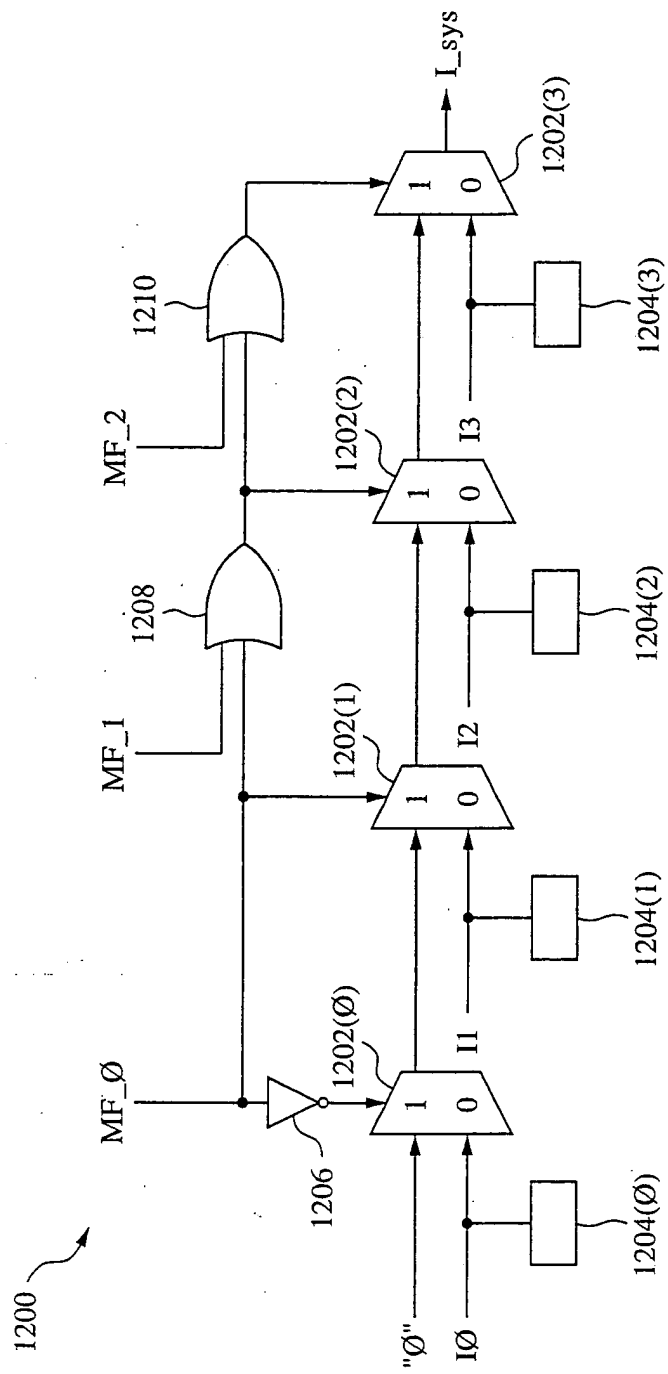


FIG. 12

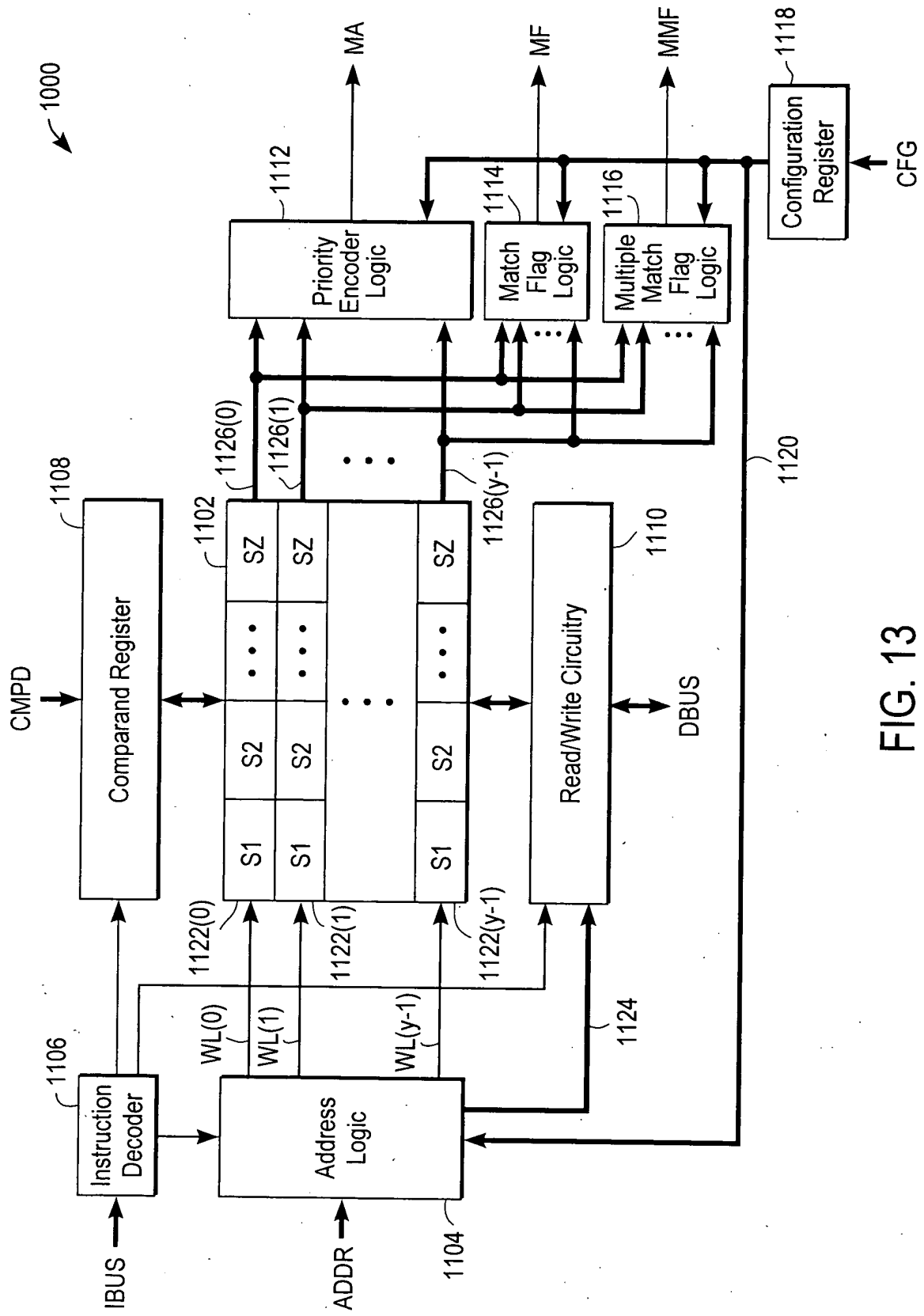


FIG. 13

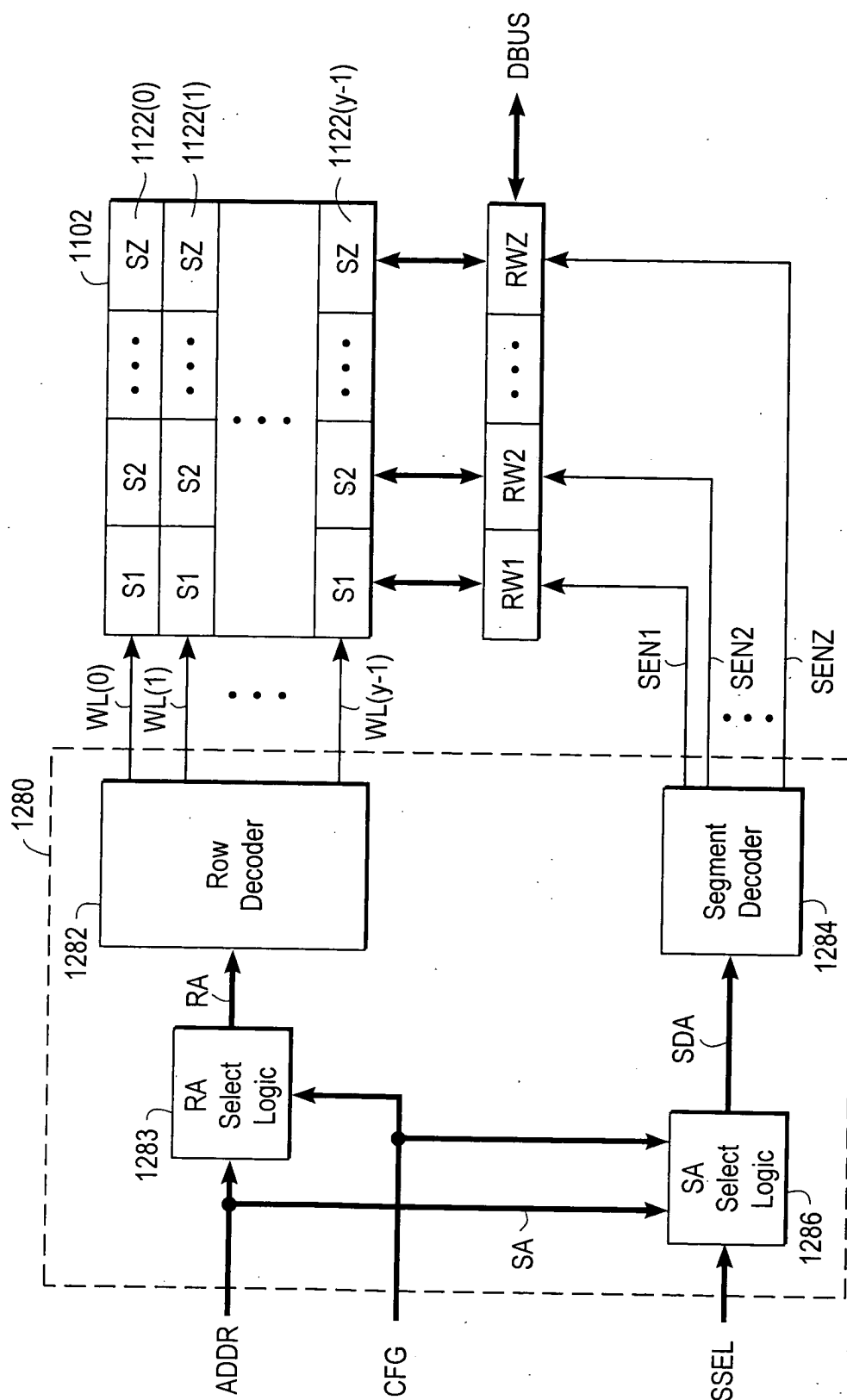


FIG. 14

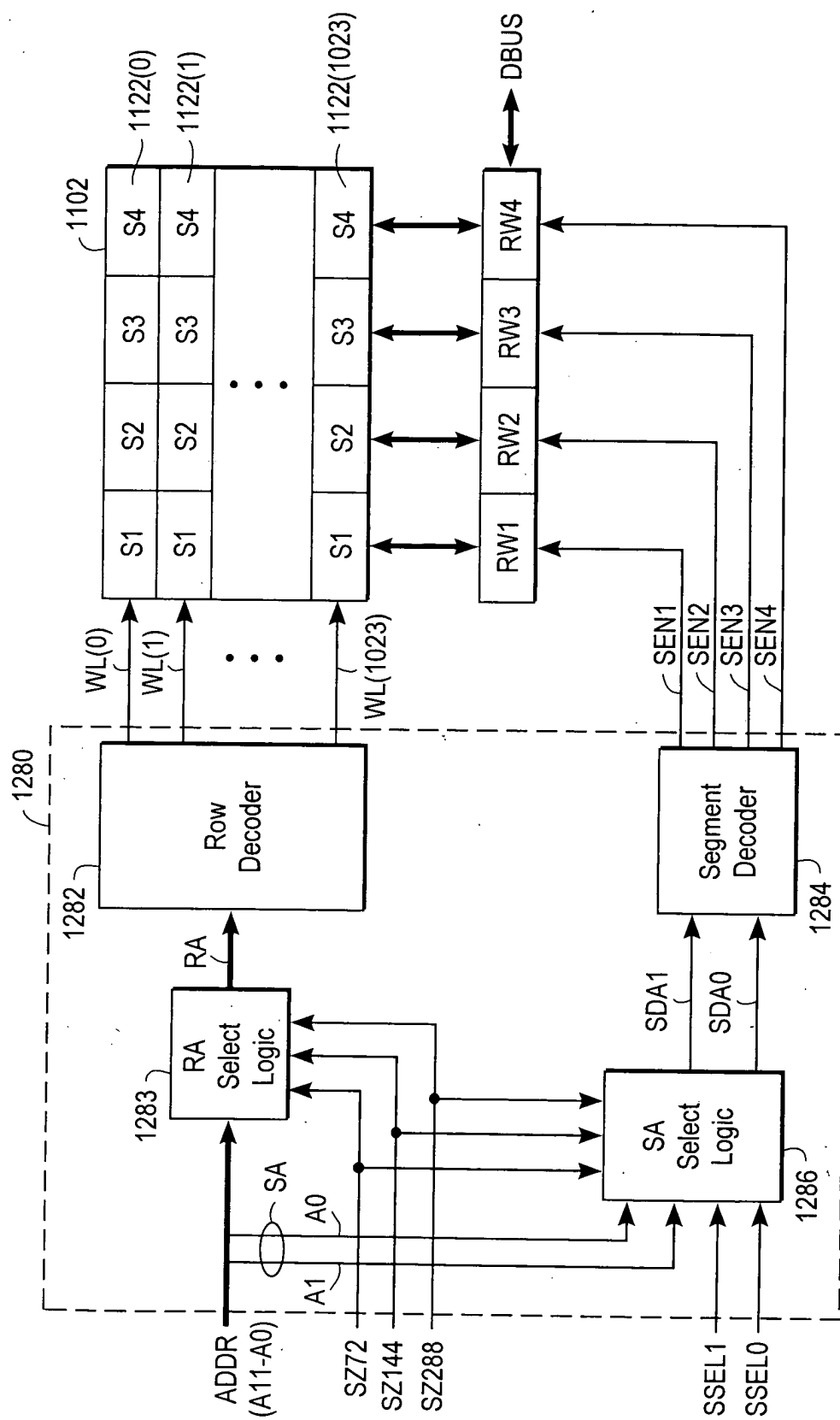


FIG. 15

CONFIG	CONFIG SIGNAL	ADDR	RA	SA	SDA
4K x 72	SZ1	A11-A0	A11-A2	A1-A0	A1-A0
2K x 144	SZG1	A10-A0	A10-A1	A0	A0, SSEL0
1K x 288	SZGZ	A9-A0	A9-A0	—	SSEL1-SSEL0

FIG. 16

CONFIG	A1	A0	SSEL1	SSEL0	SEN4	SEN3	SEN2	SEN1
4k x 72	0	0	X	X	0	0	0	1
4k x 72	0	1	X	X	0	0	1	0
4k x 72	1	0	X	X	0	1	0	0
4k x 72	1	1	X	X	1	0	0	0
2k x 144	X	0	X	0	0	0	0	1
2k x 144	X	0	X	1	0	0	1	0
2k x 144	X	1	X	0	0	1	0	0
2k x 144	X	1	X	1	1	0	0	0
1k x 288	X	X	0	0	0	0	0	1
1k x 288	X	X	0	1	0	0	1	0
1k x 288	X	X	1	0	0	1	0	0
1k x 288	X	X	1	1	1	0	0	0

FIG. 17

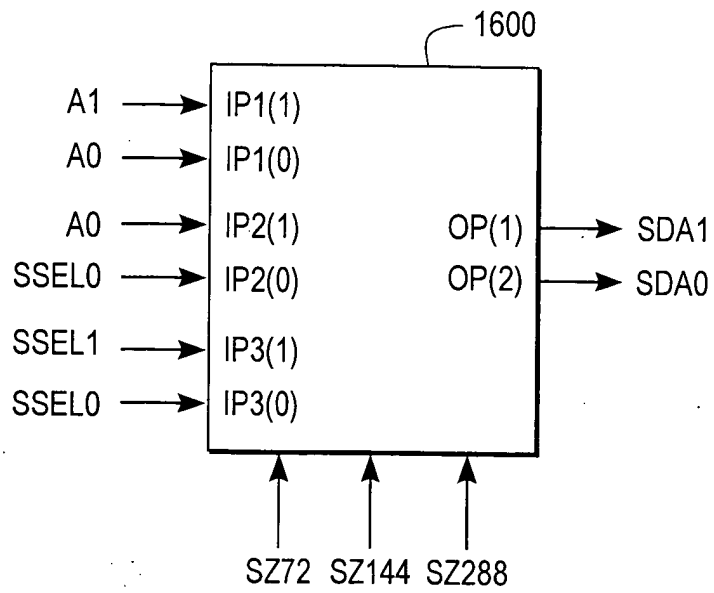


FIG. 18A

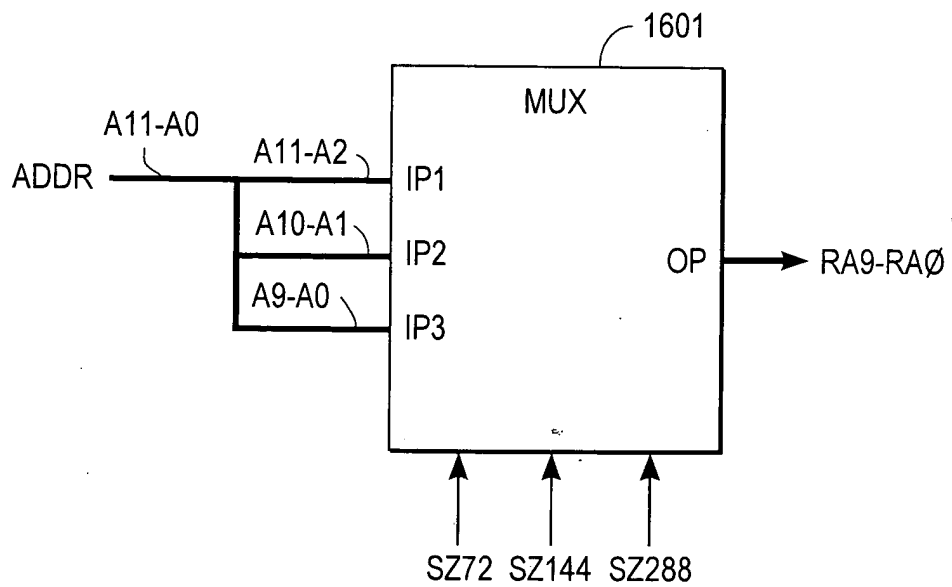


FIG. 18B

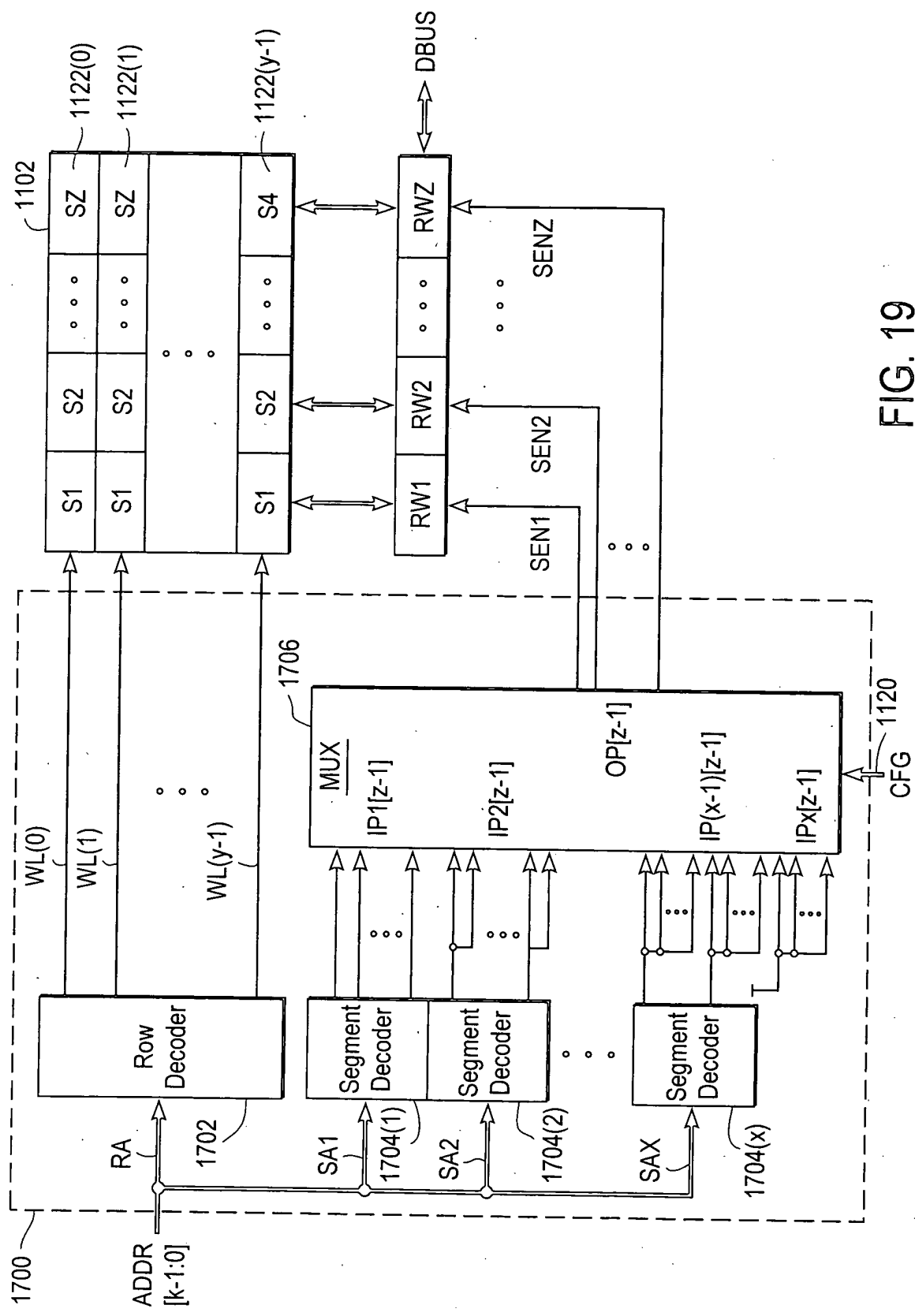


FIG. 19

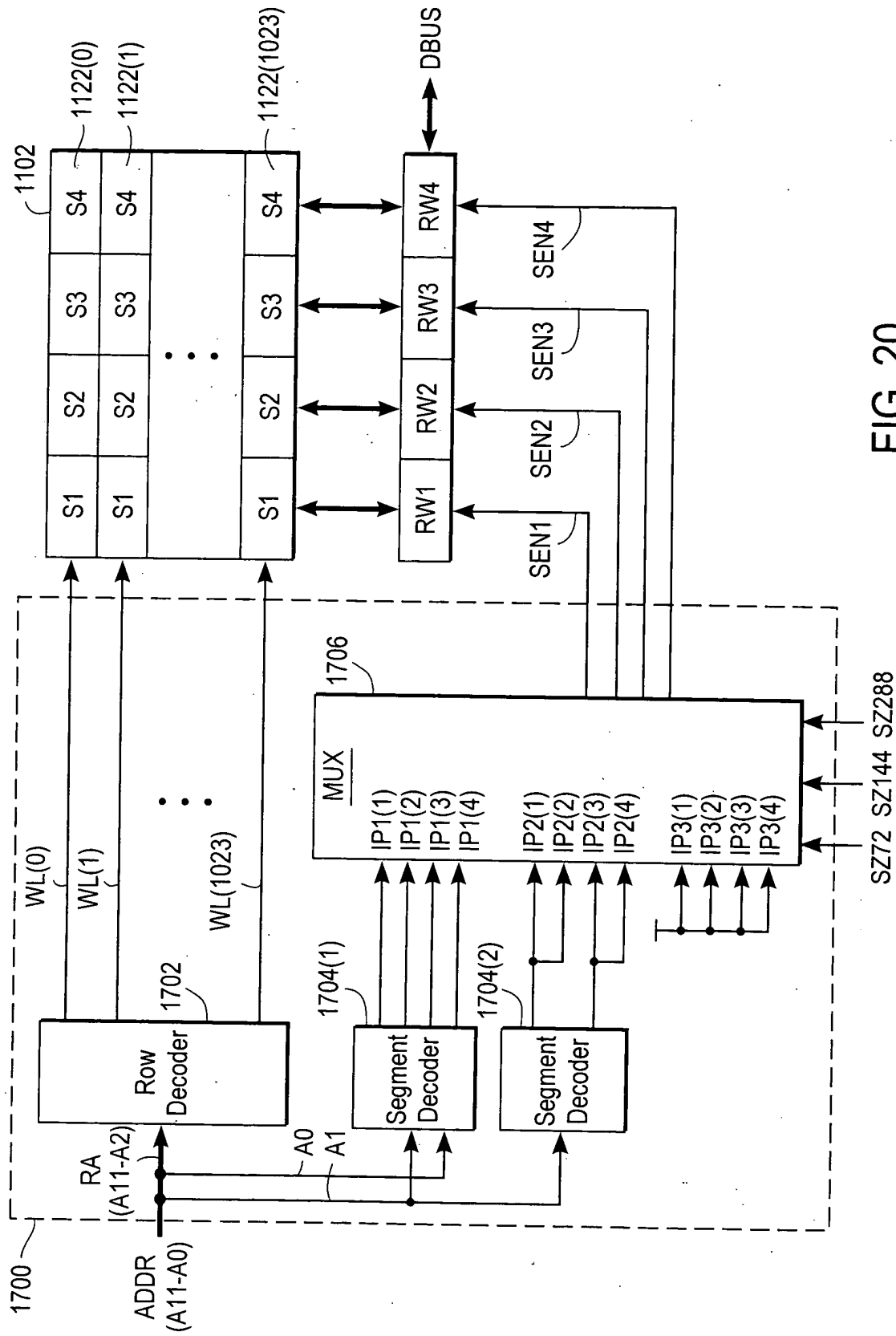


FIG. 20

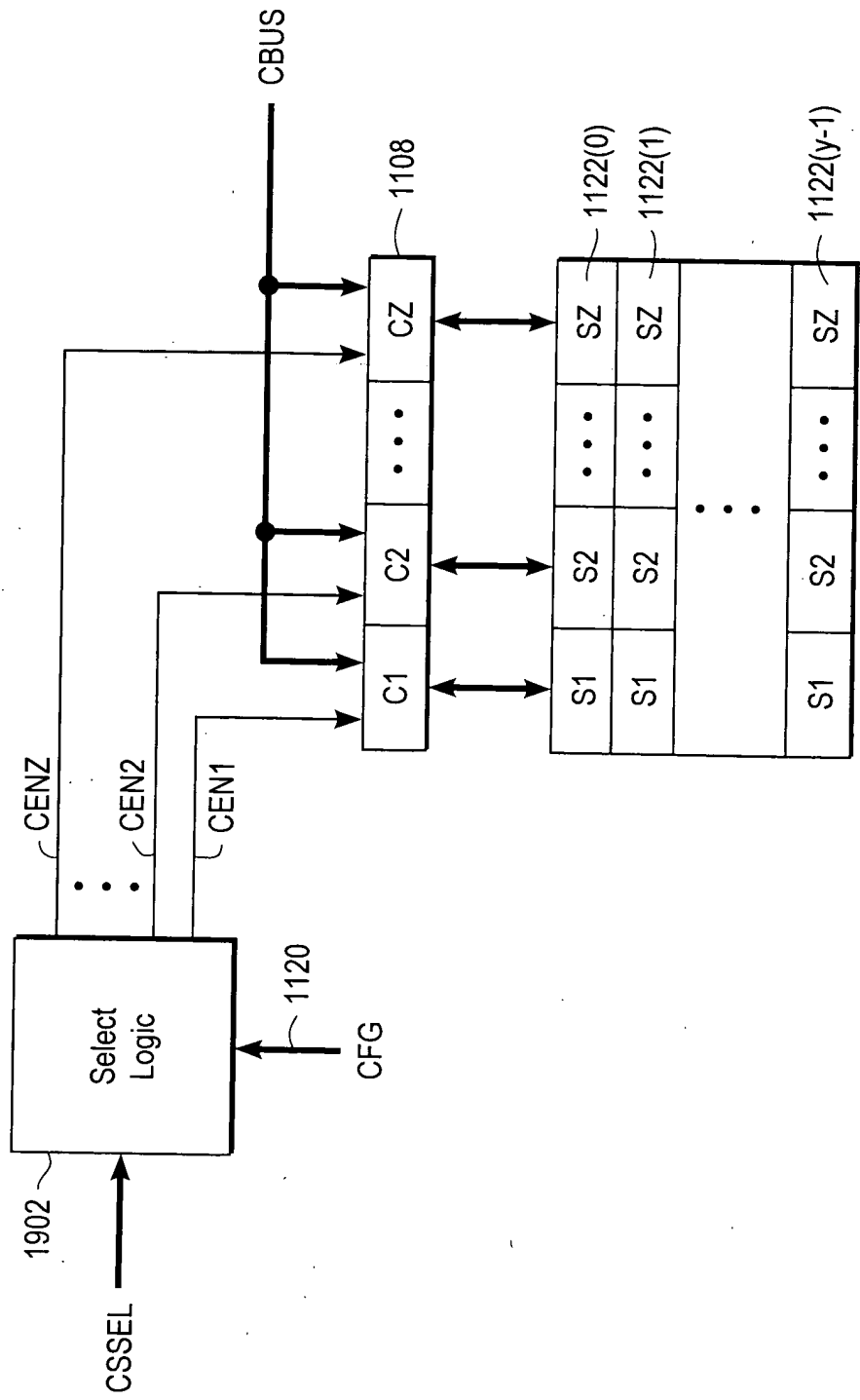


FIG. 21

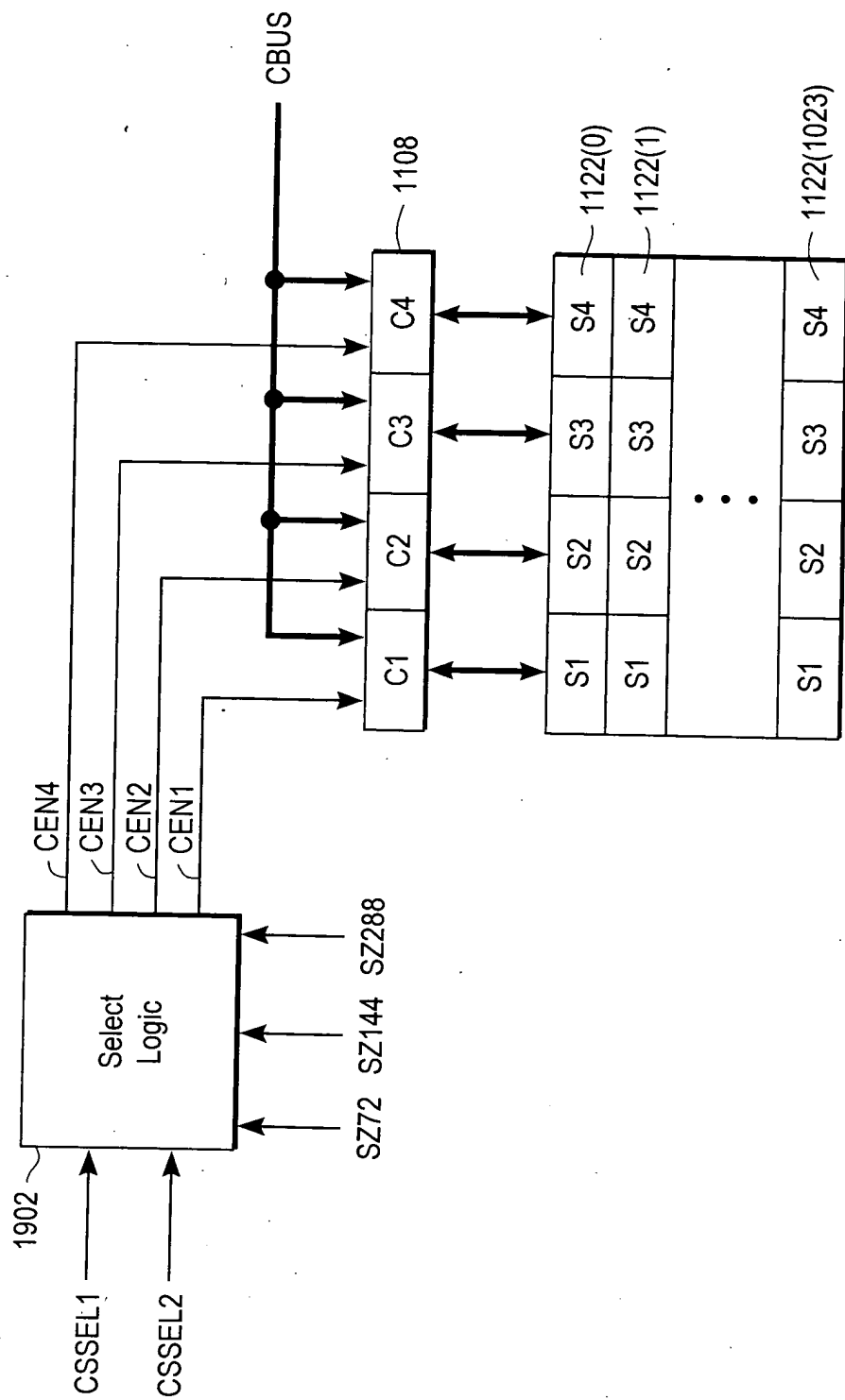


FIG. 22

CONFIG	CSSEL1	CSSEL0	CEN1	CEN2	CEN3	CEN4
4k x 72	X	X	1	1	1	1
2k x 144	X	0	1	0	1	0
2k x 144	X	1	0	1	0	1
1k x 288	0	0	1	0	0	0
1k x 288	0	1	0	1	0	0
1k x 288	1	0	0	0	1	0
1k x 288	1	1	0	0	0	1

FIG. 23

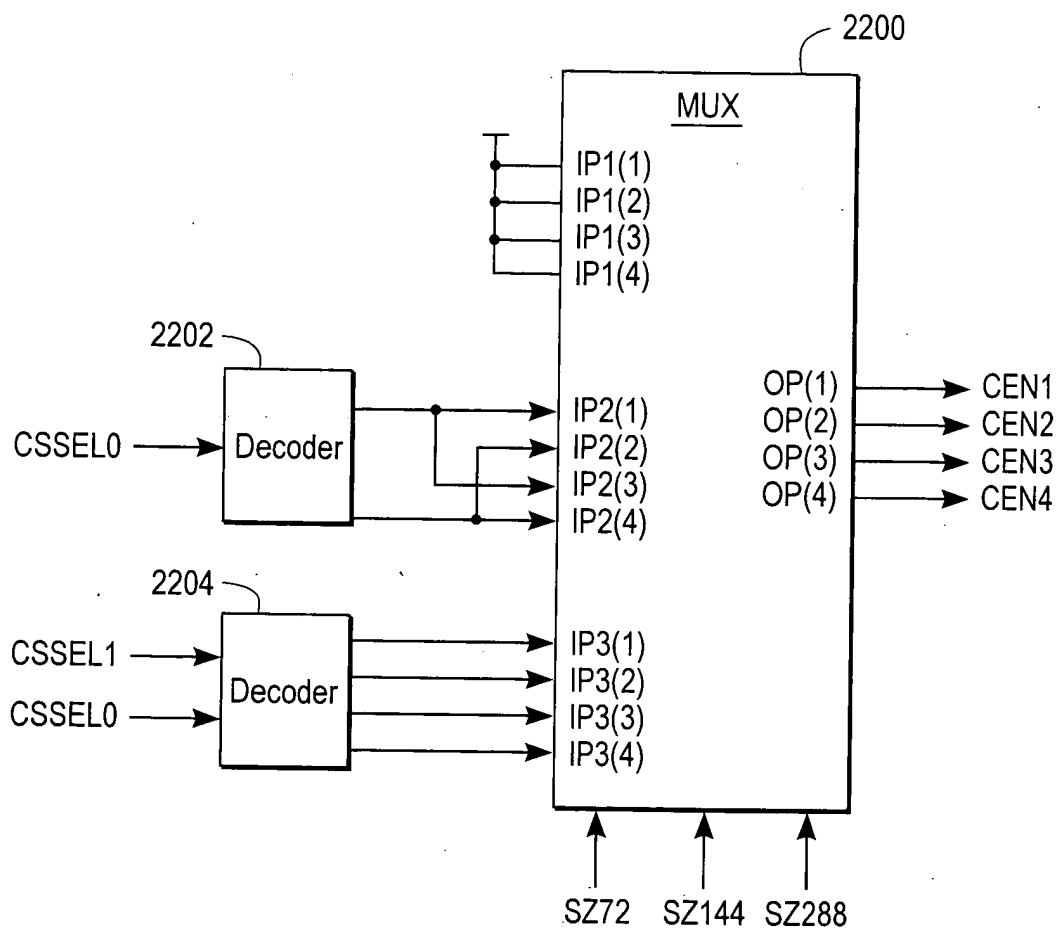


FIG. 24

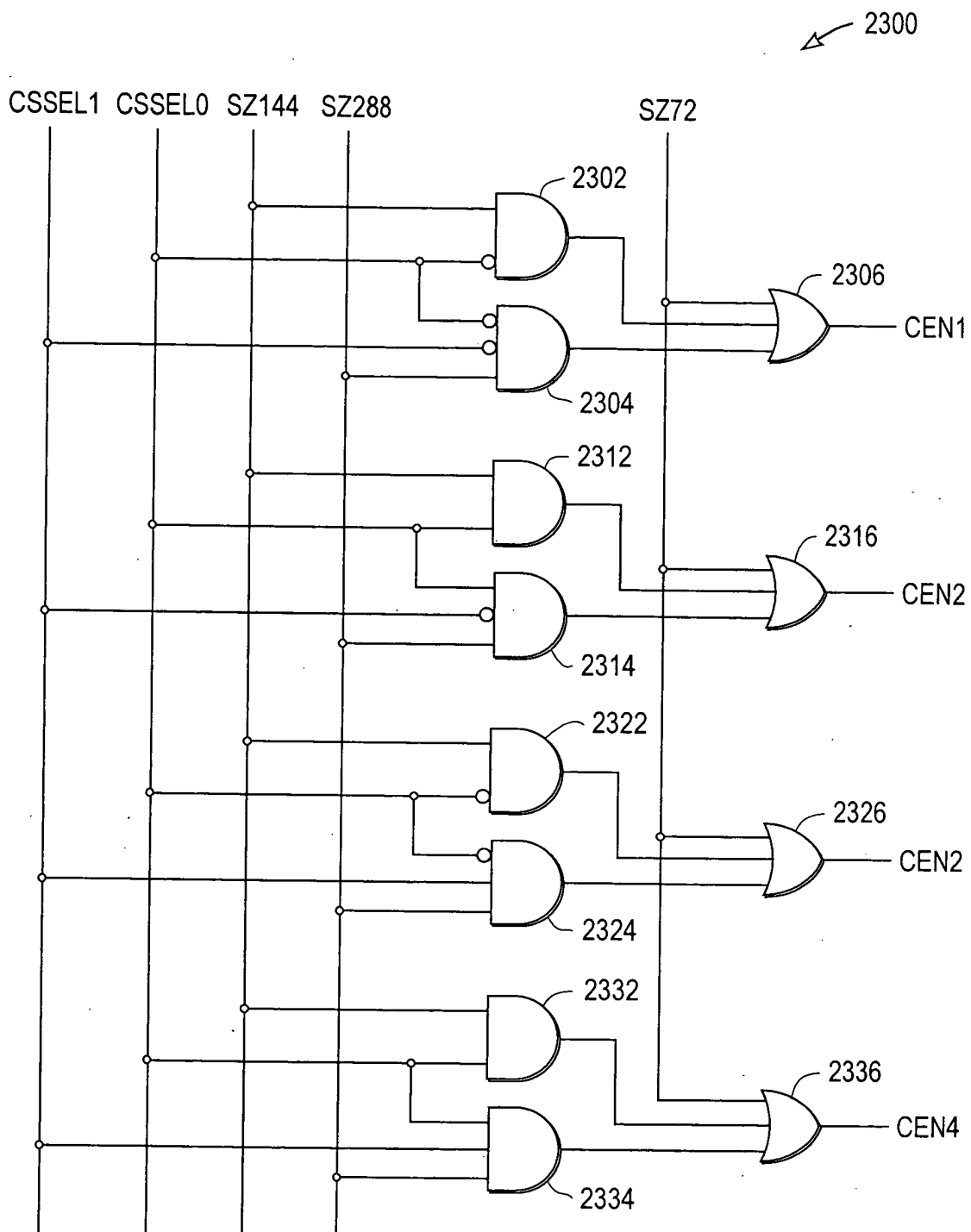


FIG. 25

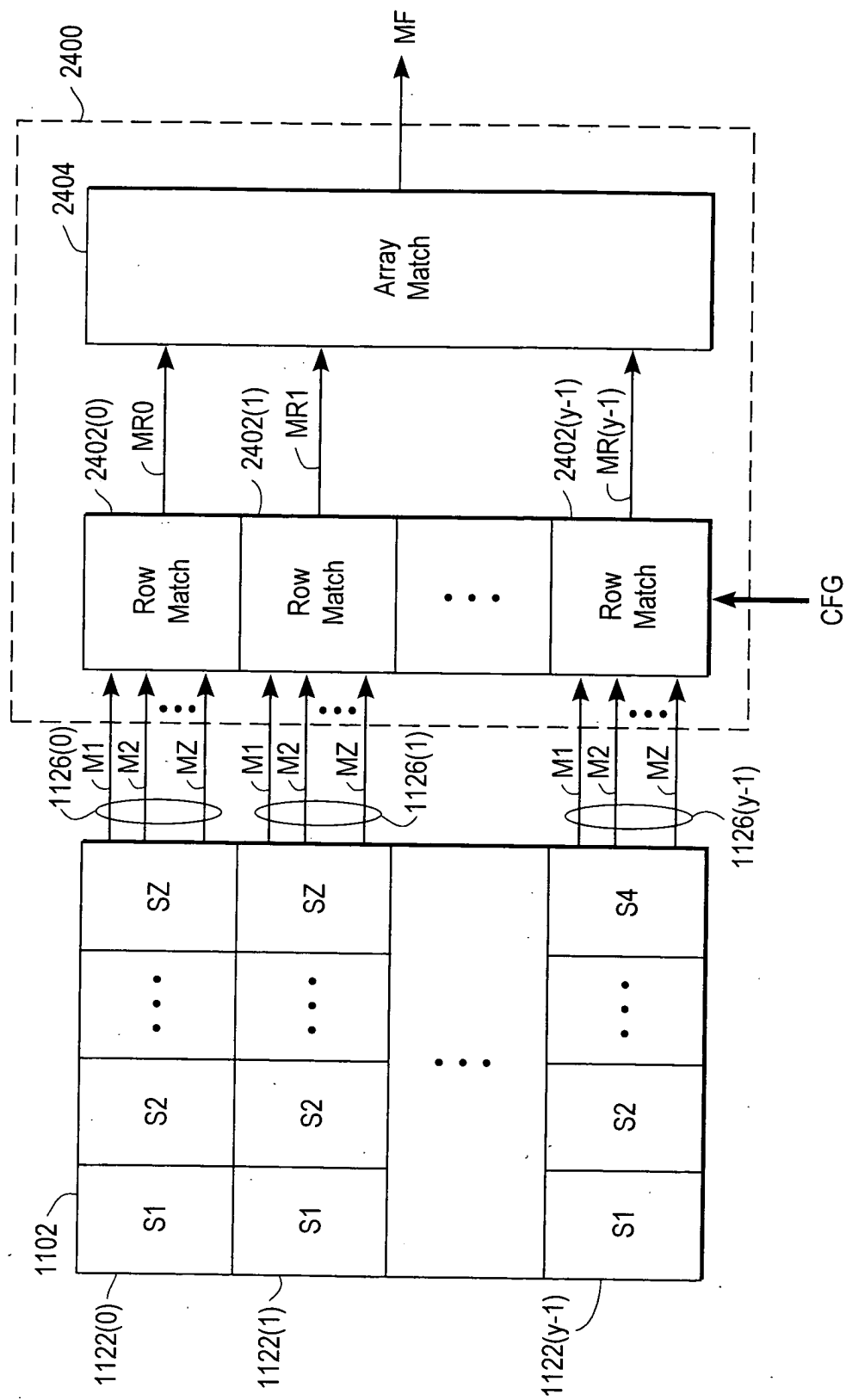


FIG. 26

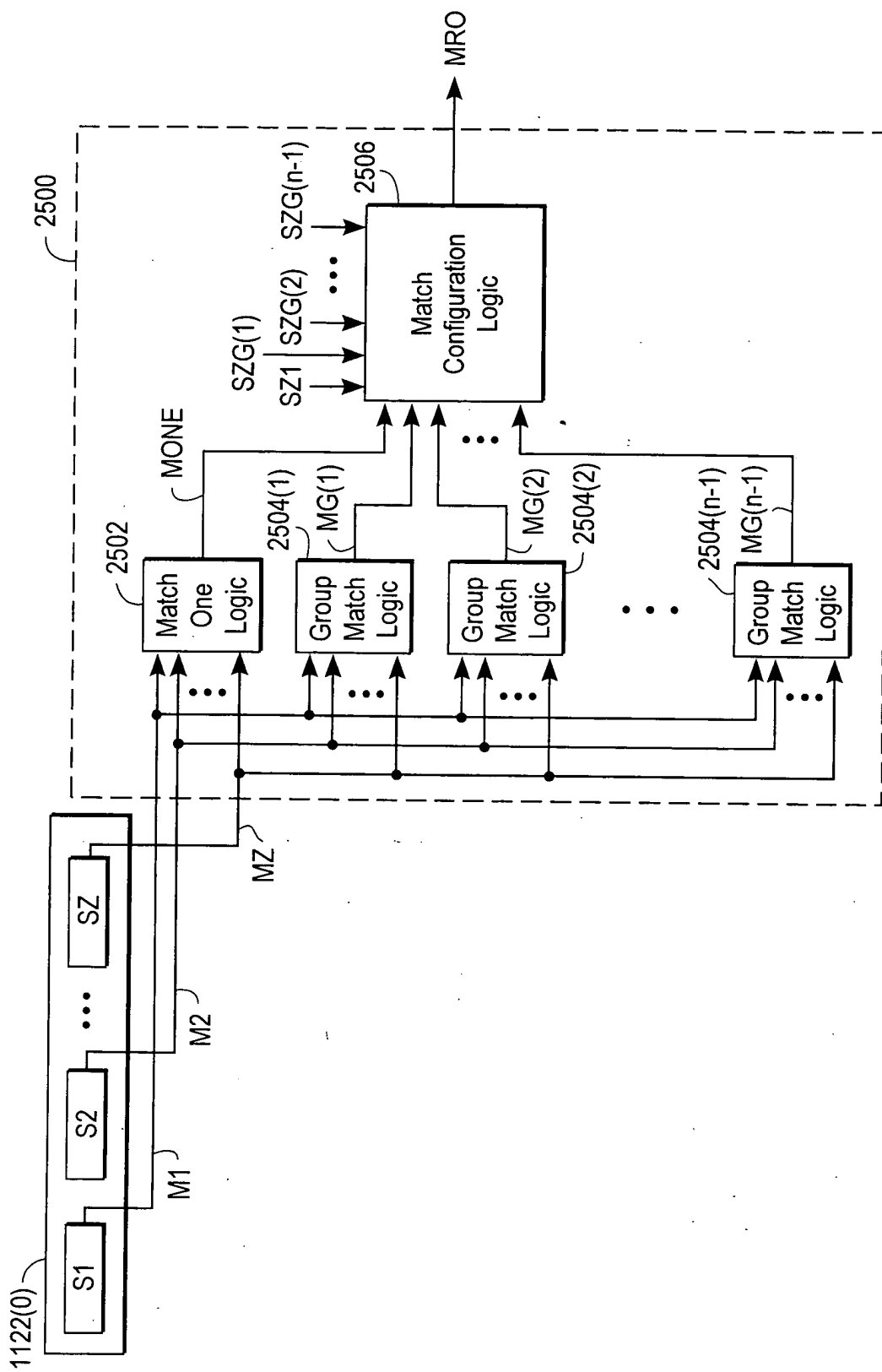


FIG. 27

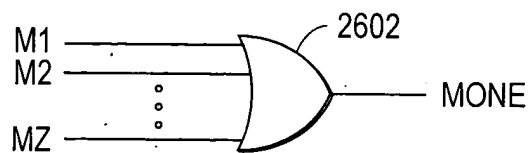


FIG. 28

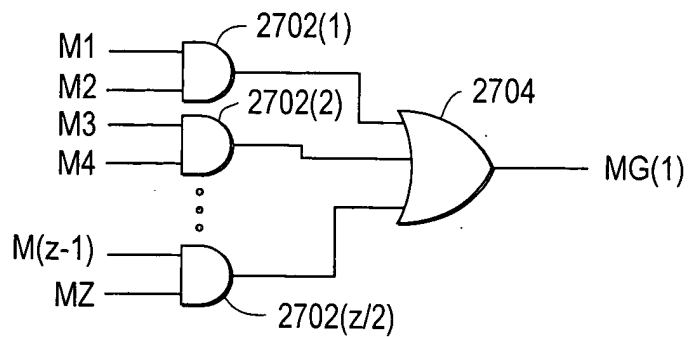


FIG. 29A

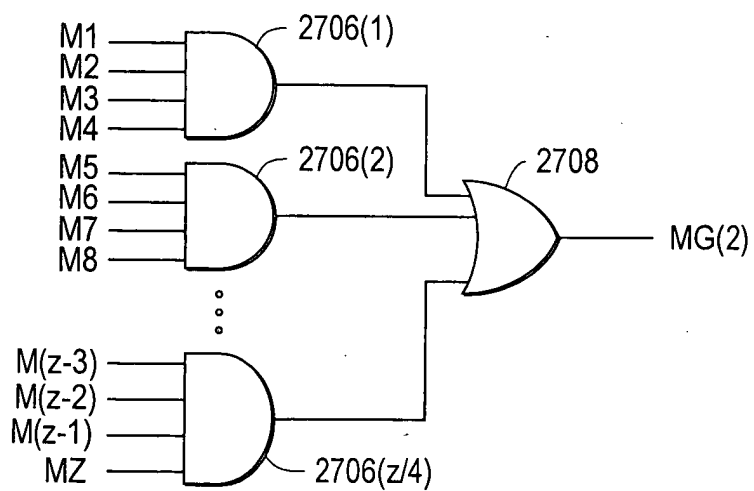


FIG. 29B

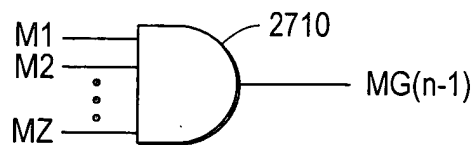


FIG. 29C

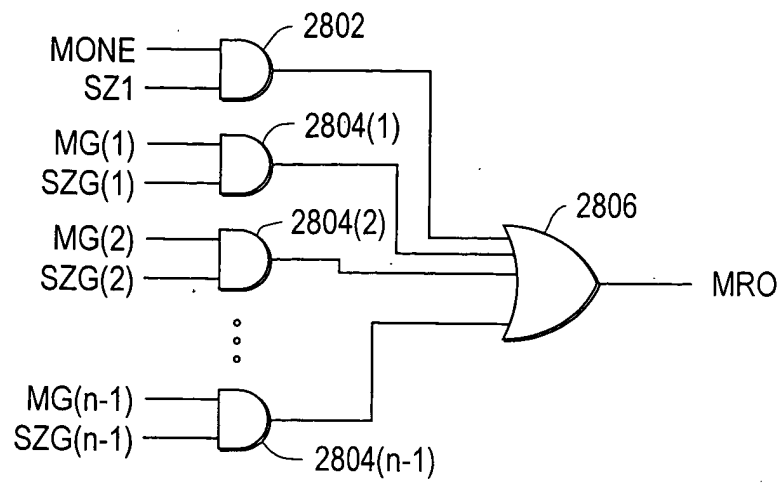


FIG. 30

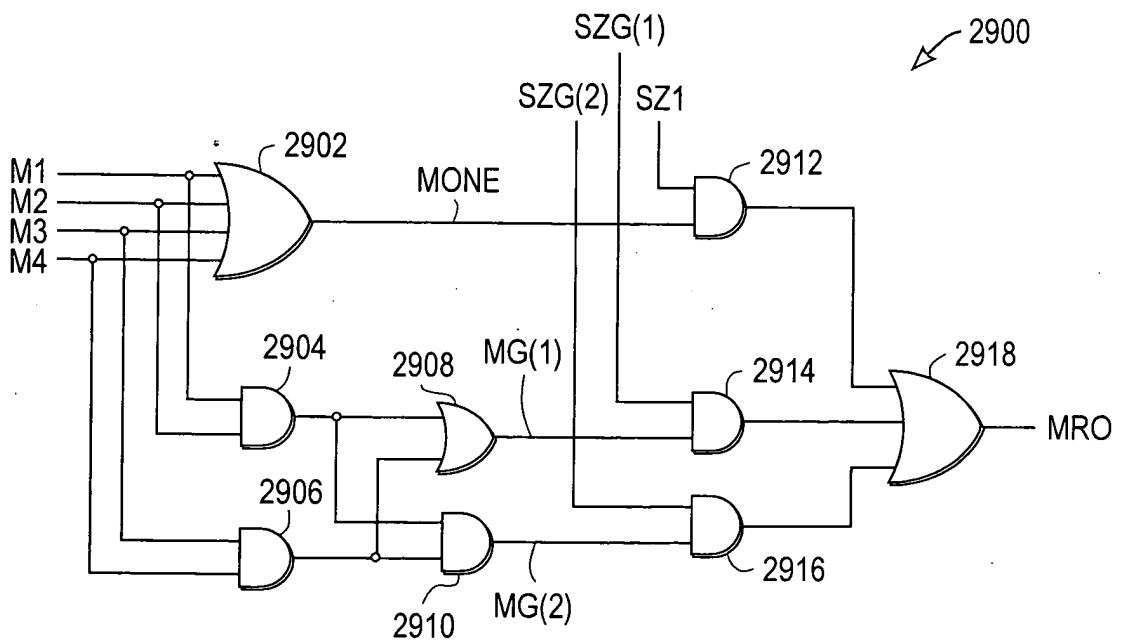


FIG. 31

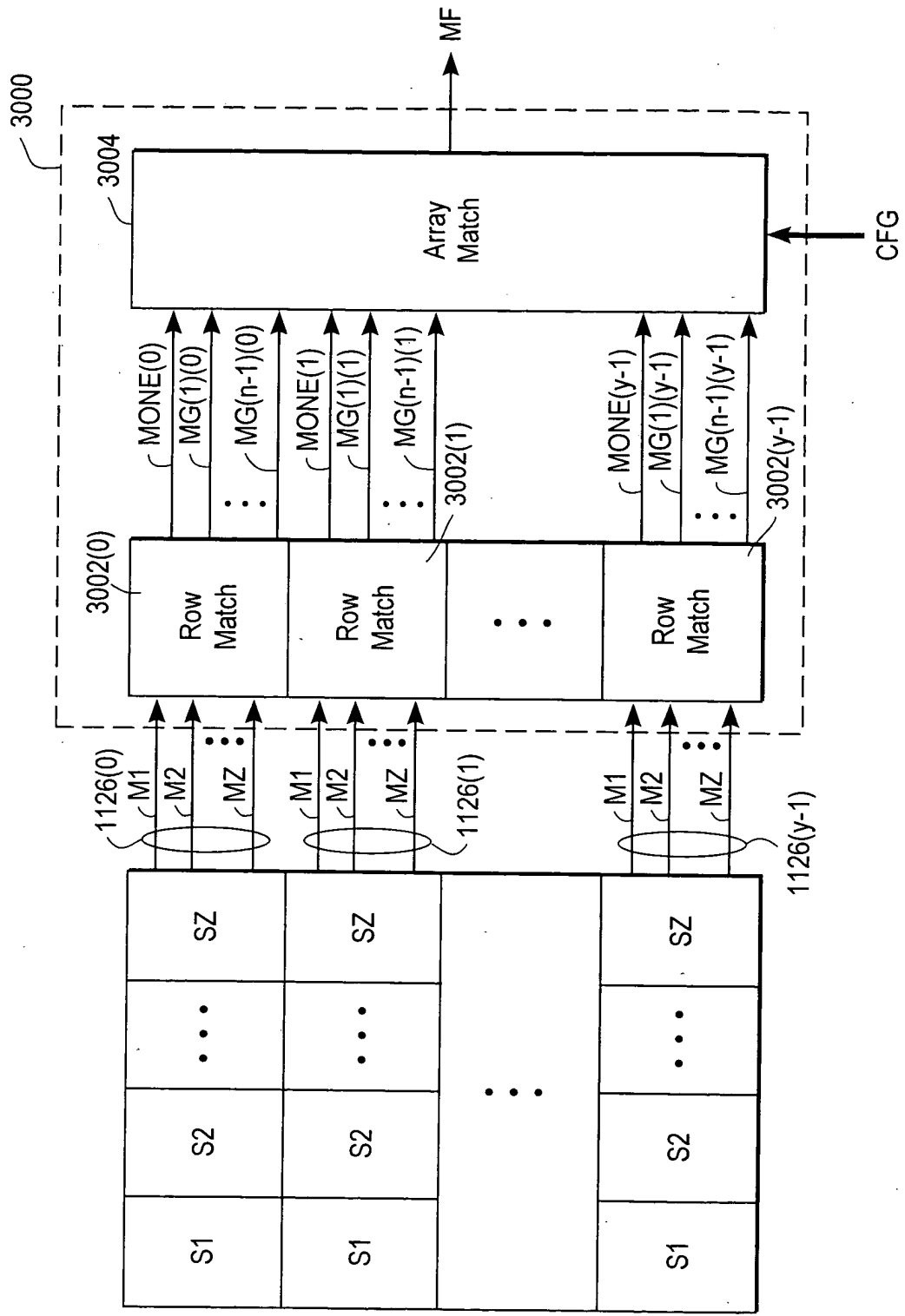


FIG. 32

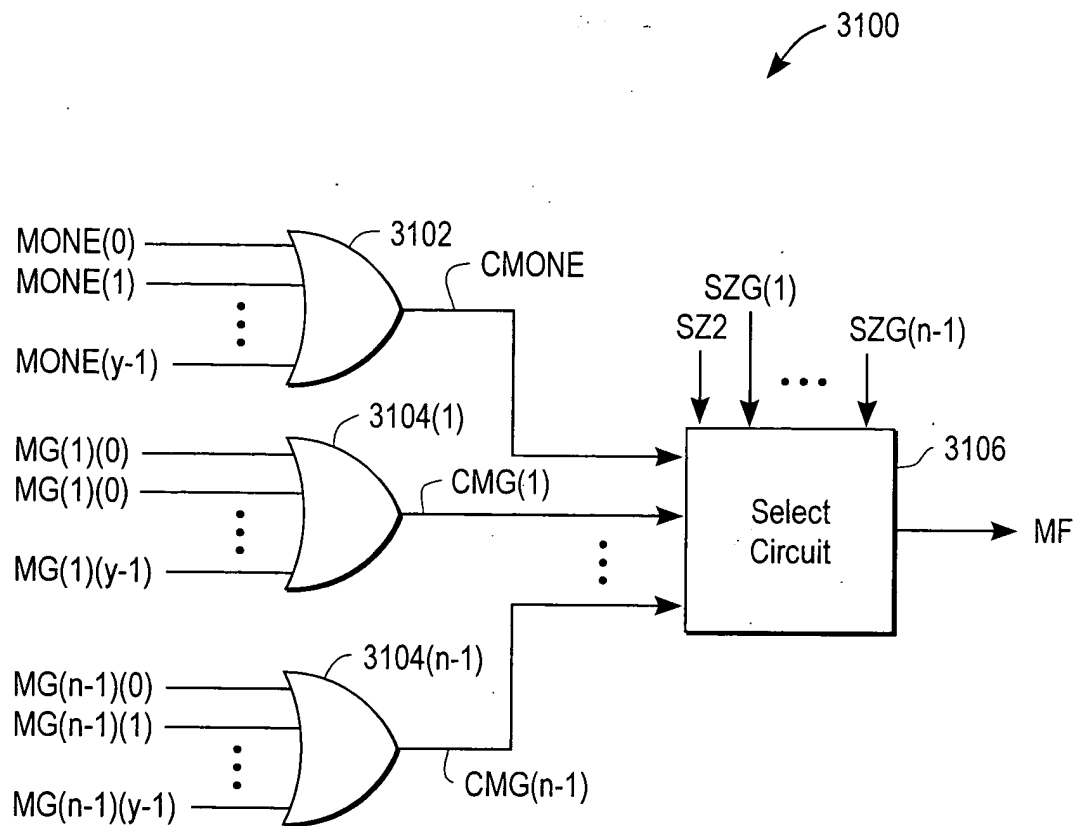


FIG. 33

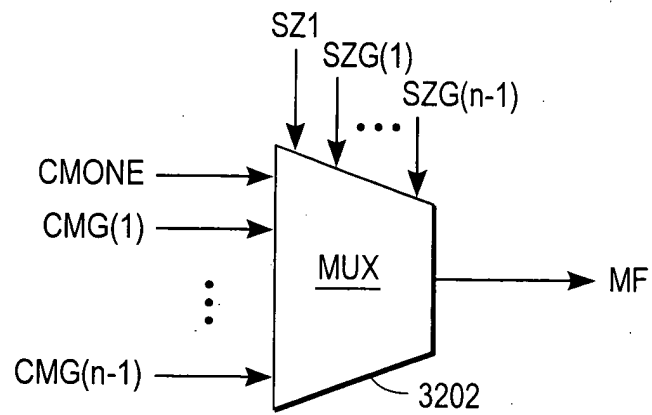


FIG. 34

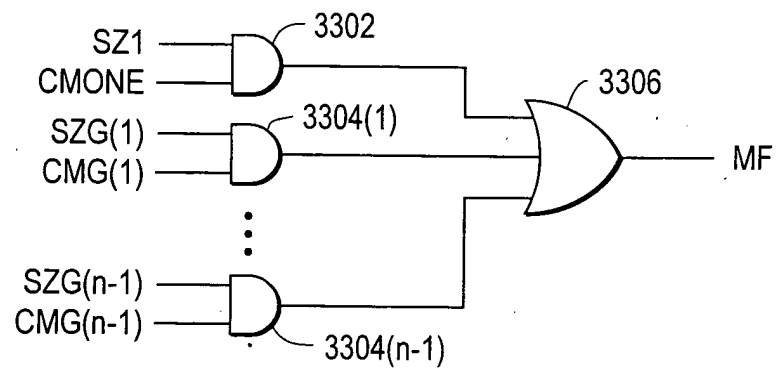


FIG. 35

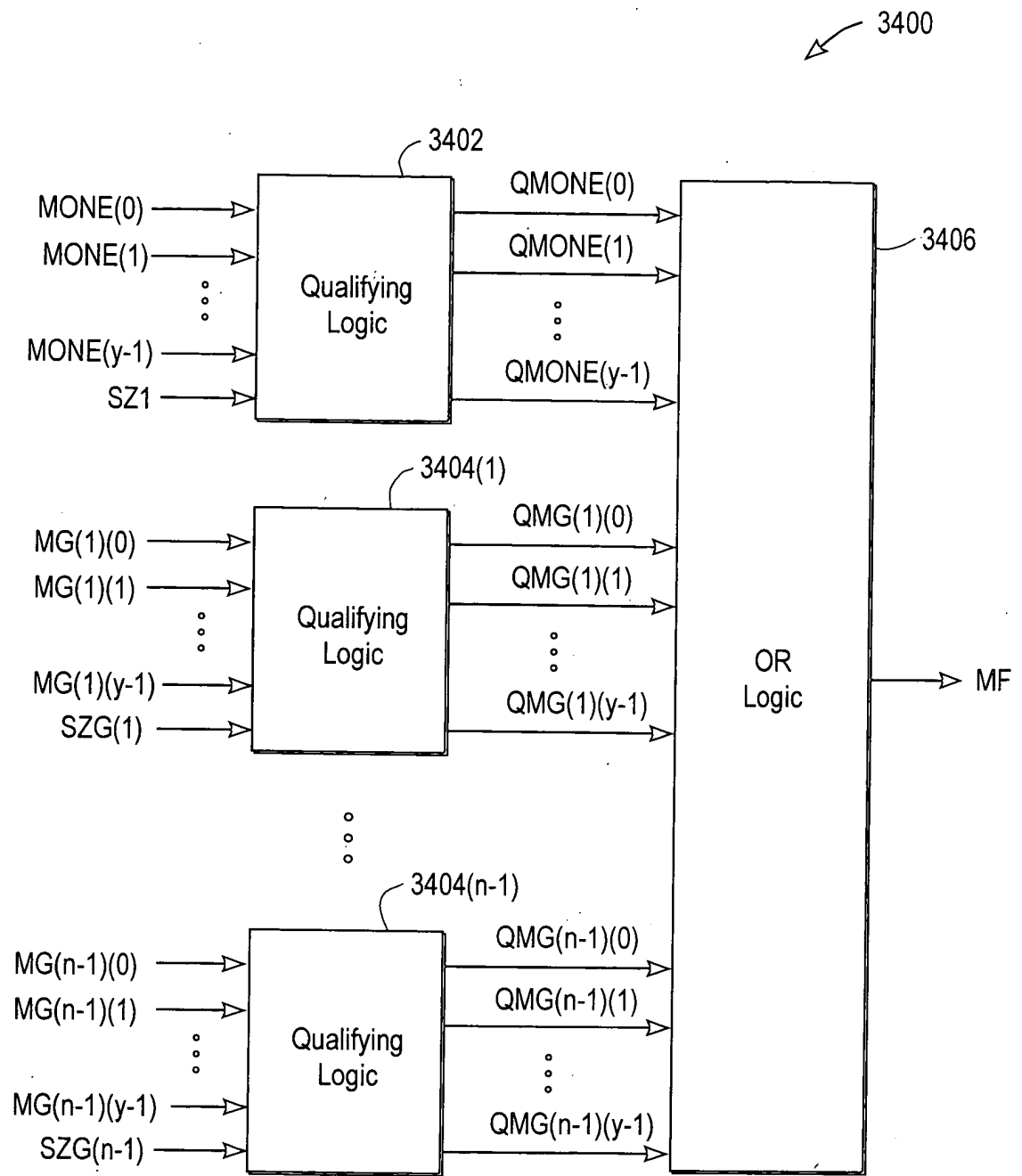


FIG. 36

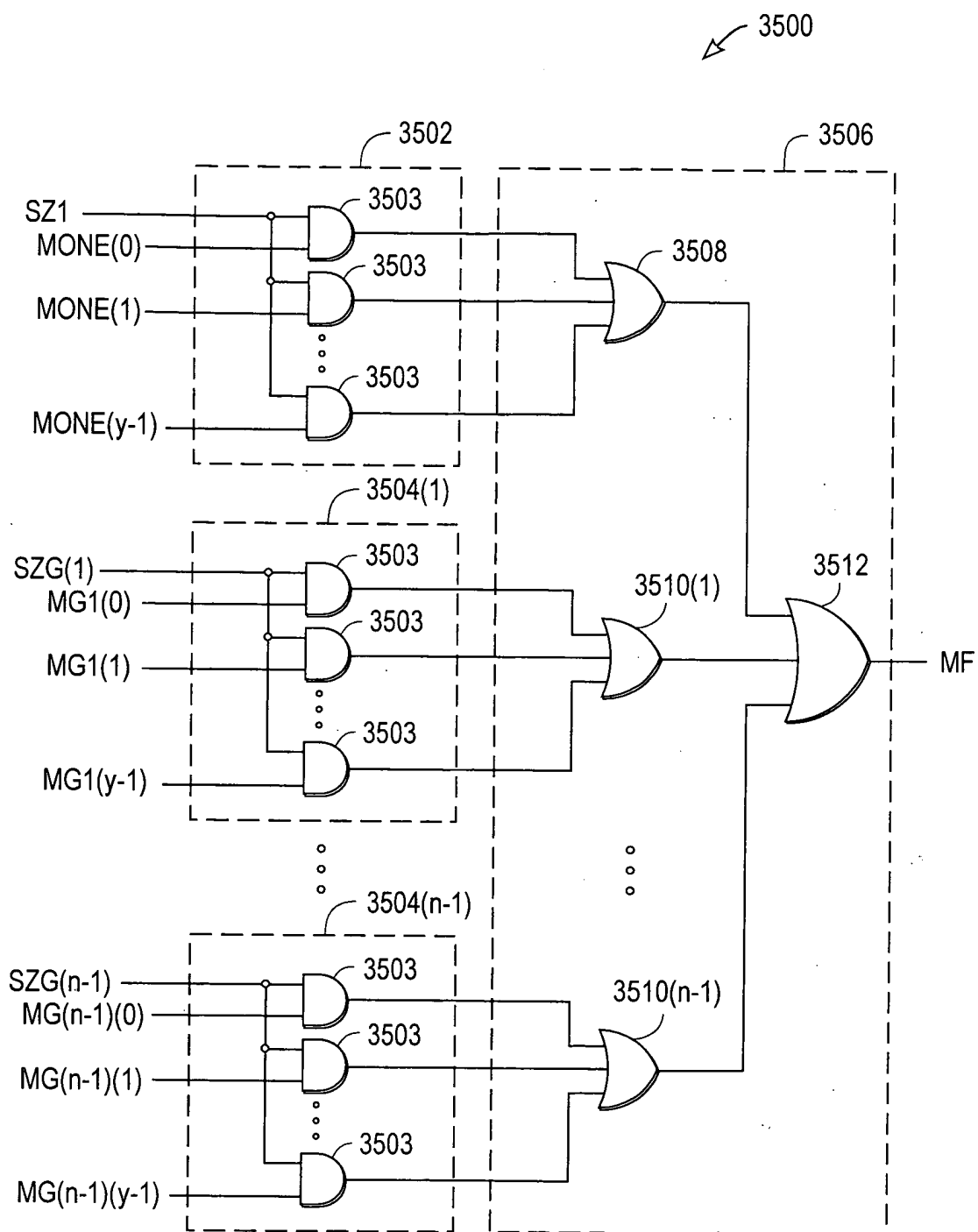


FIG. 37

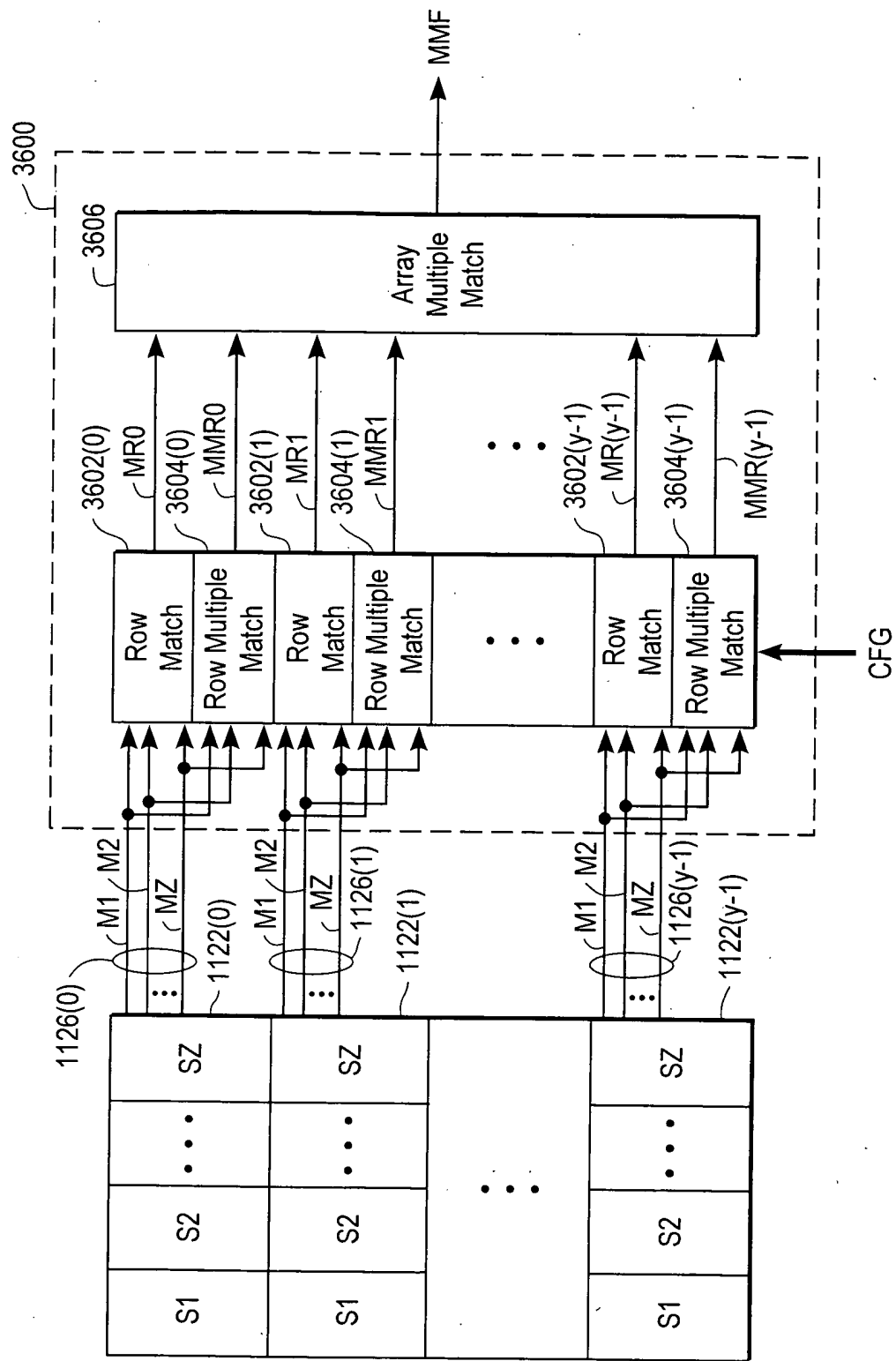


FIG. 38

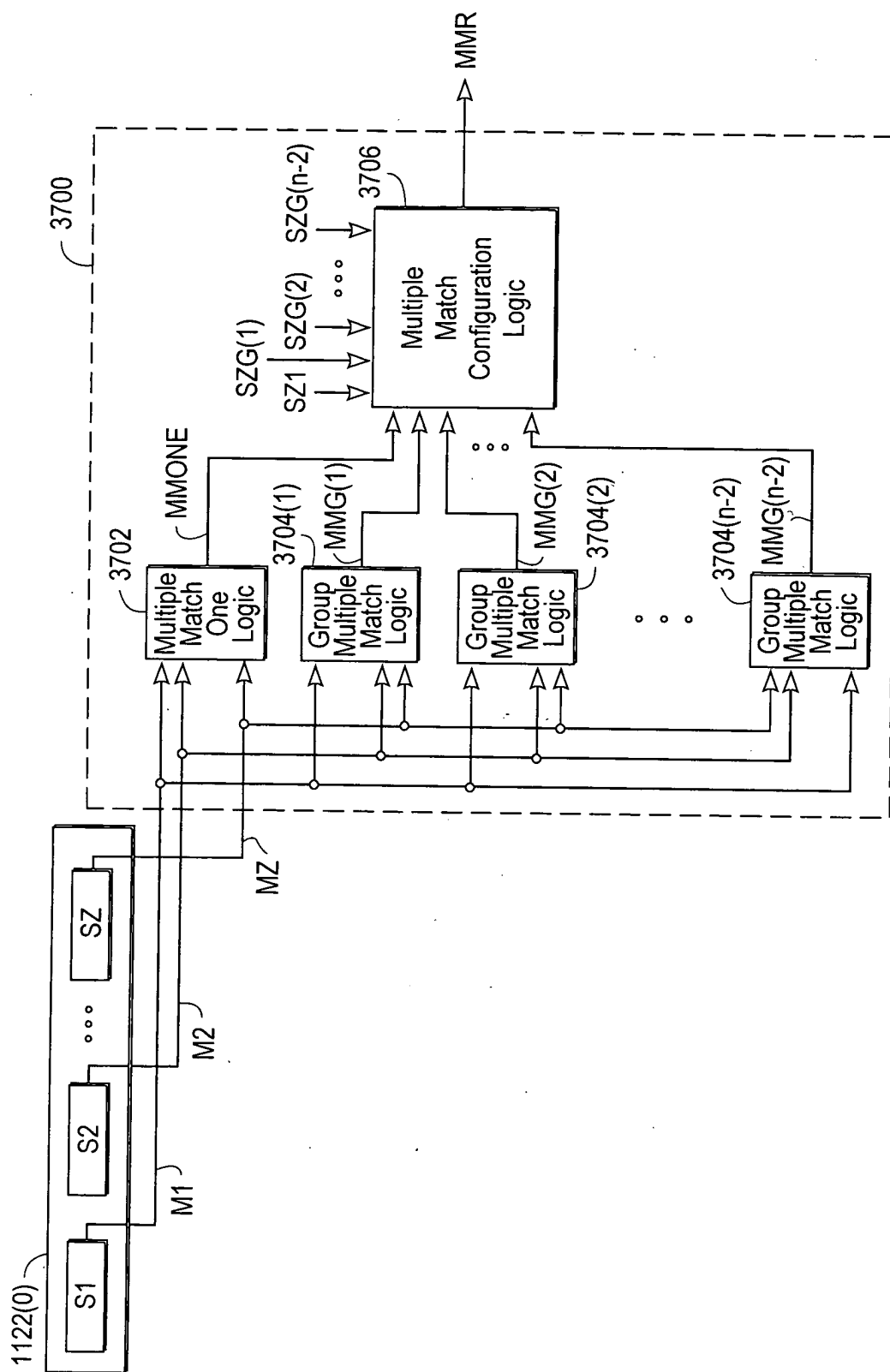


FIG. 39

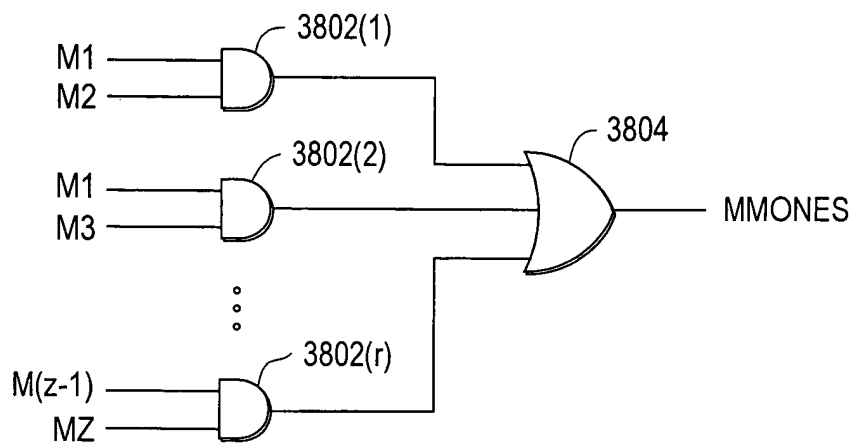


FIG. 40

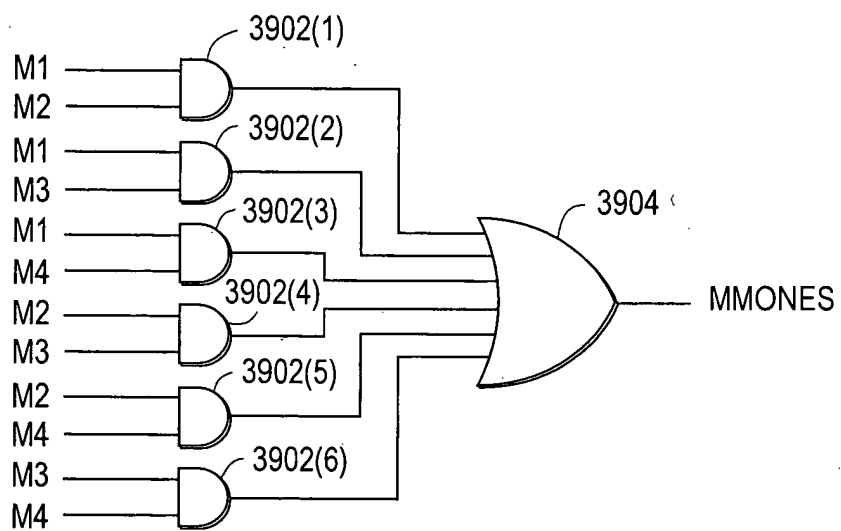


FIG. 41

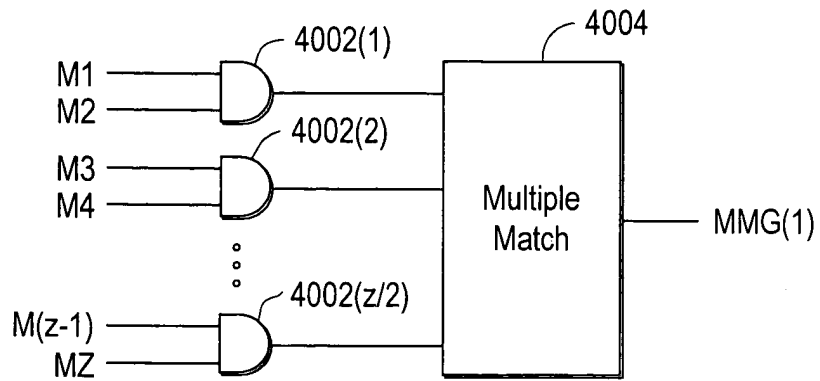


FIG. 42A

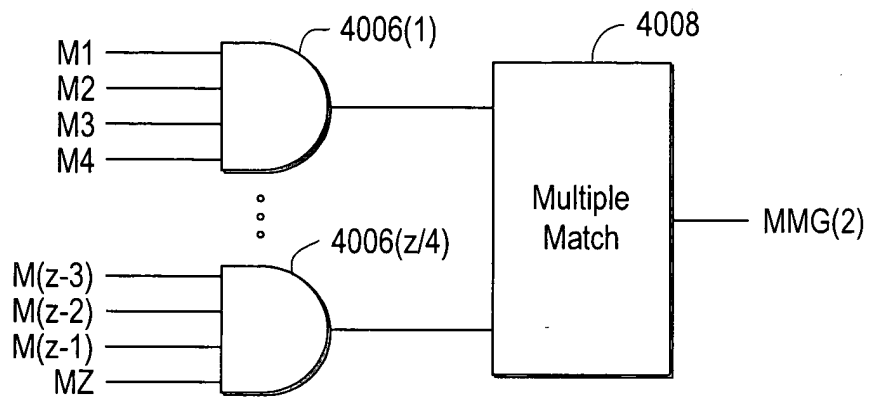


FIG. 42B

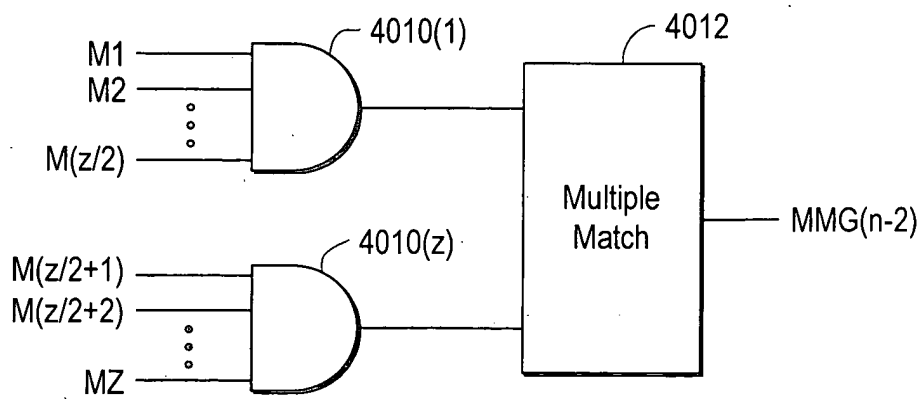


FIG. 42C

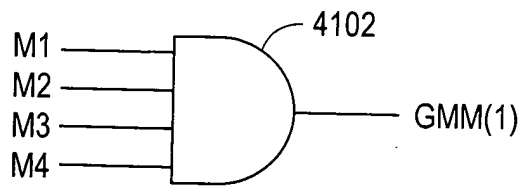


FIG. 43

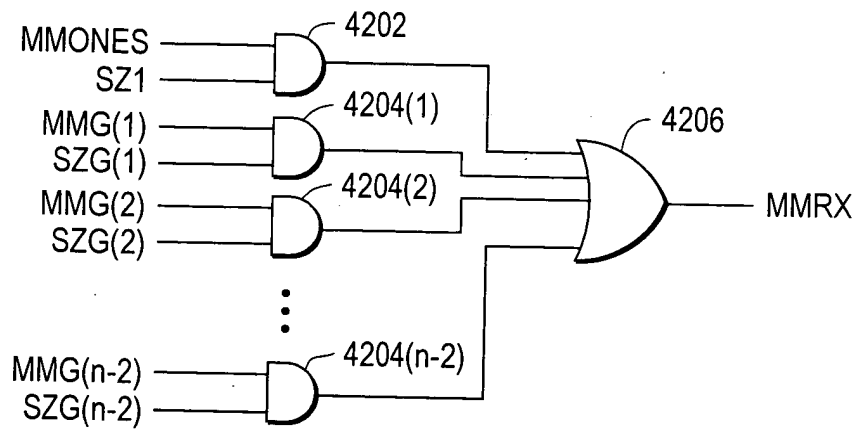


FIG. 44

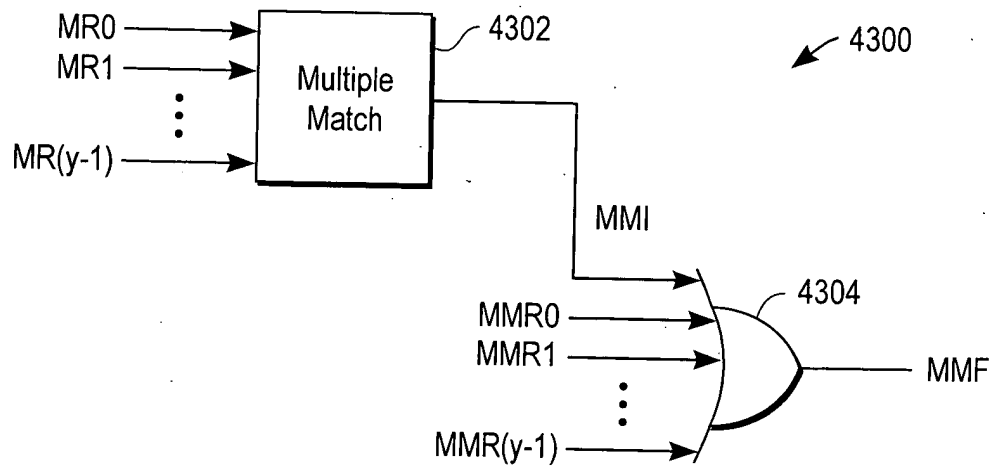
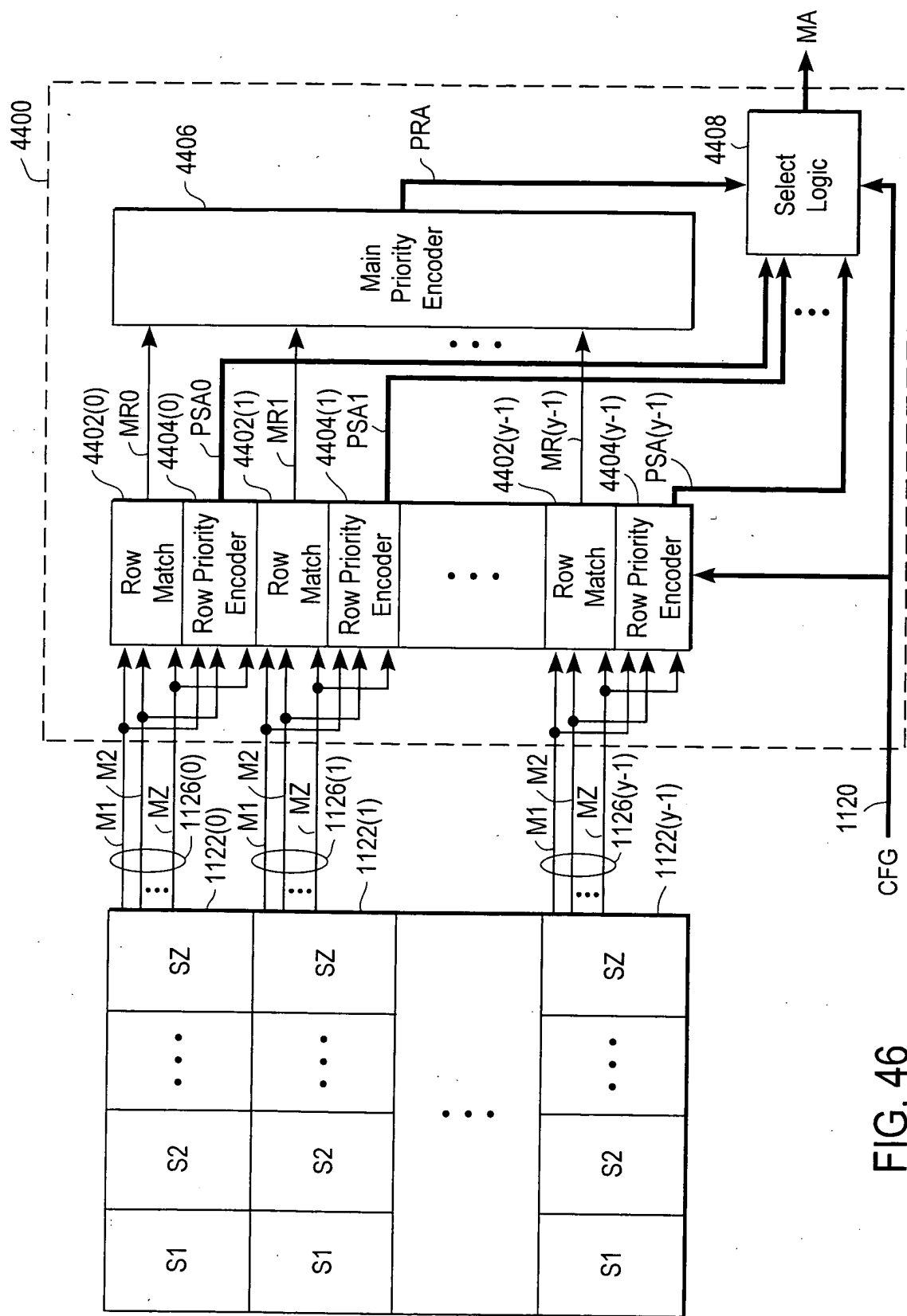


FIG. 45



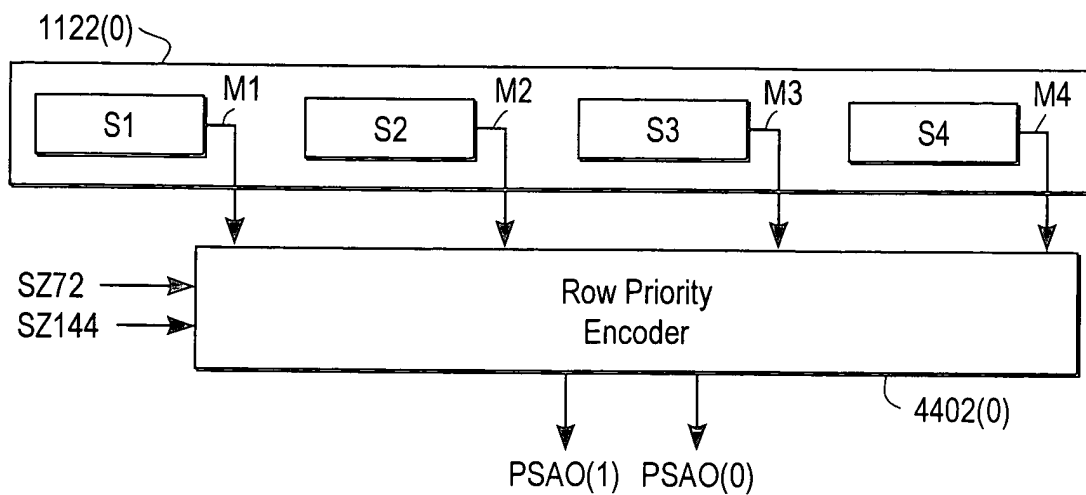


FIG. 47

M1	M2	M3	M4	ADDR	PSAO(1)	PSAO(0)
0	0	0	0	X	X	X
0	0	0	1	3	1	1
0	0	1	0	2	1	0
0	0	1	1	2	1	0
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0

FIG. 48

M1	M2	M3	M4	ADDR	PSAO(1)	PSAO(0)
0	0	0	0	X	X	X
0	0	0	1	0	X	X
0	0	1	0	0	X	X
0	0	1	1	1	1	X
0	1	0	0	0	X	X
0	1	0	1	0	X	X
0	1	1	0	0	X	X
0	1	1	1	1	1	X
1	0	0	0	0	X	X
1	0	0	1	0	X	X
1	0	1	0	0	X	X
1	0	1	1	1	1	X
1	1	0	0	0	0	X
1	1	0	1	0	0	X
1	1	1	0	0	0	X
1	1	1	1	0	0	X
1	1	1	1	0	0	X

FIG. 49

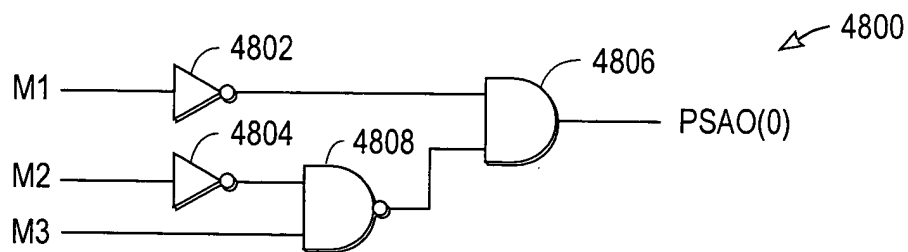


FIG. 50

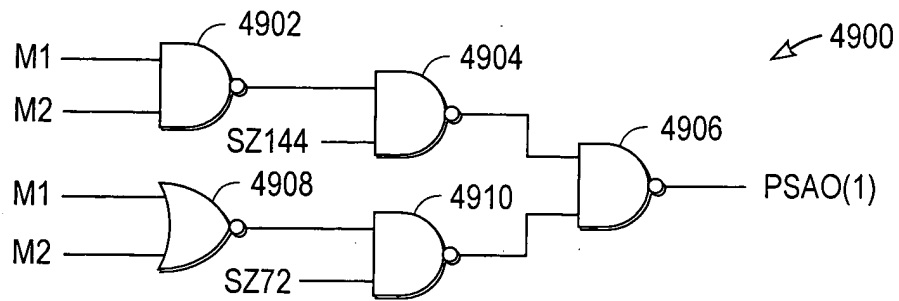


FIG. 51

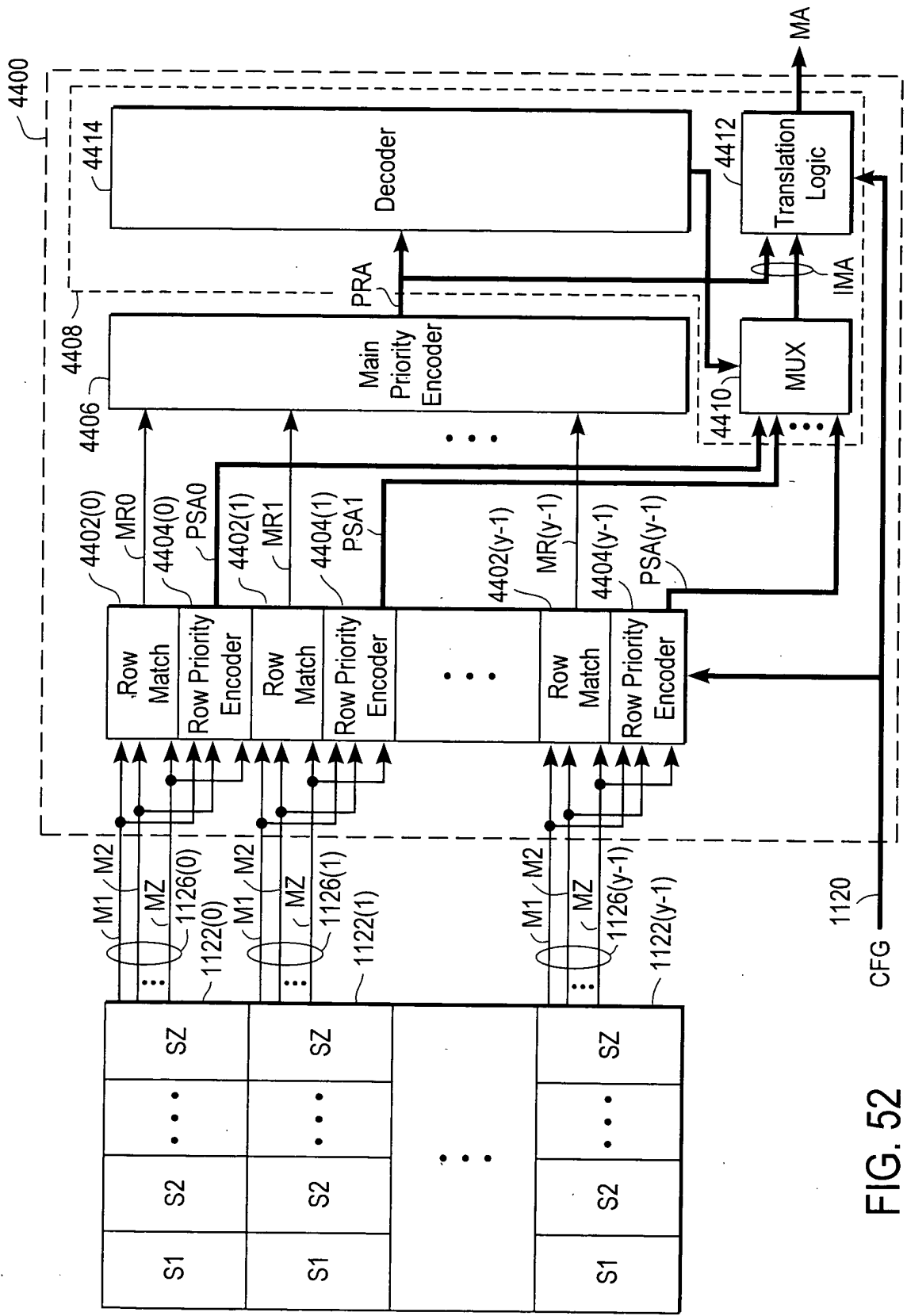


FIG. 52

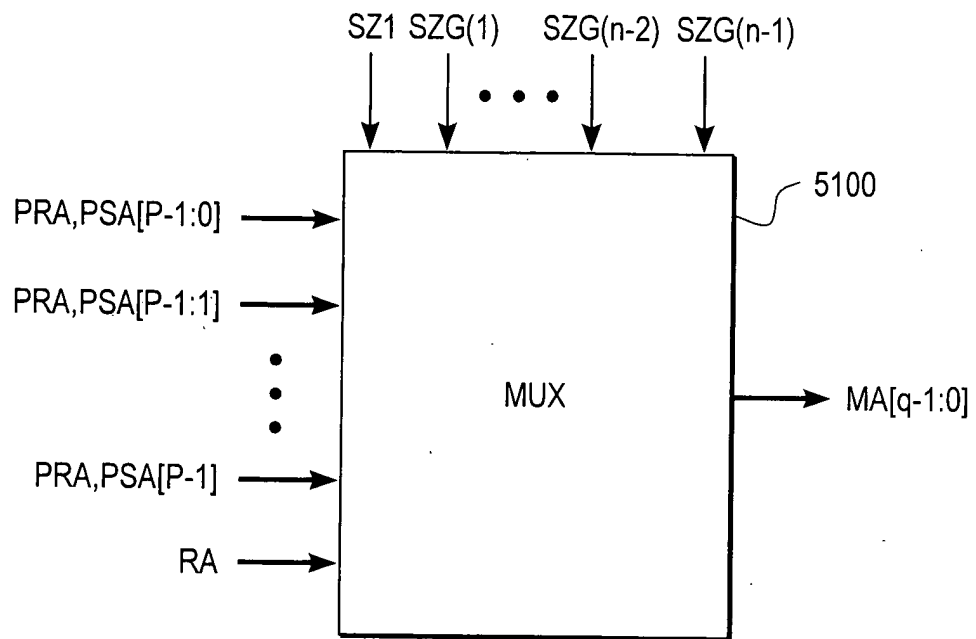


FIG. 53

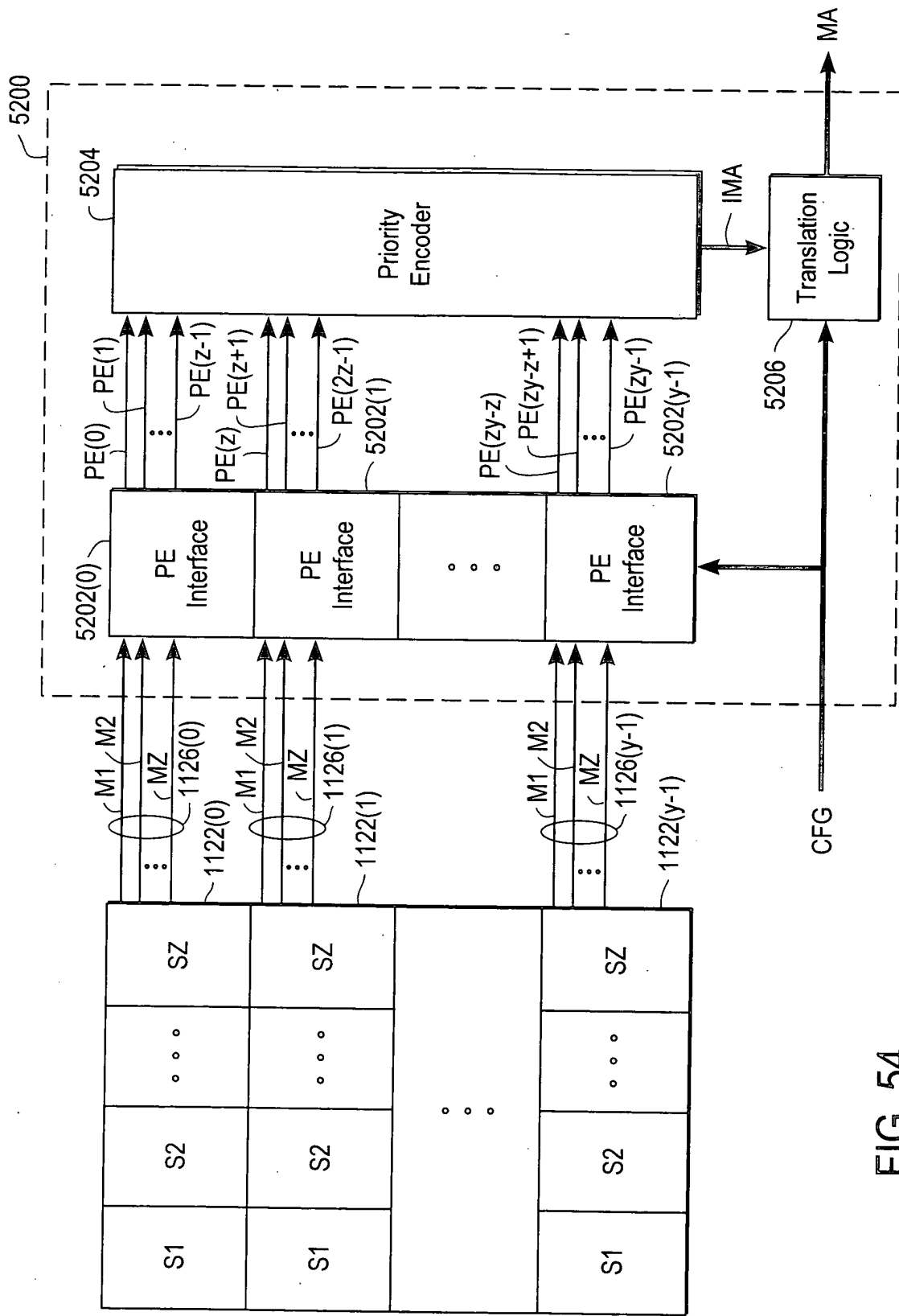


FIG. 54

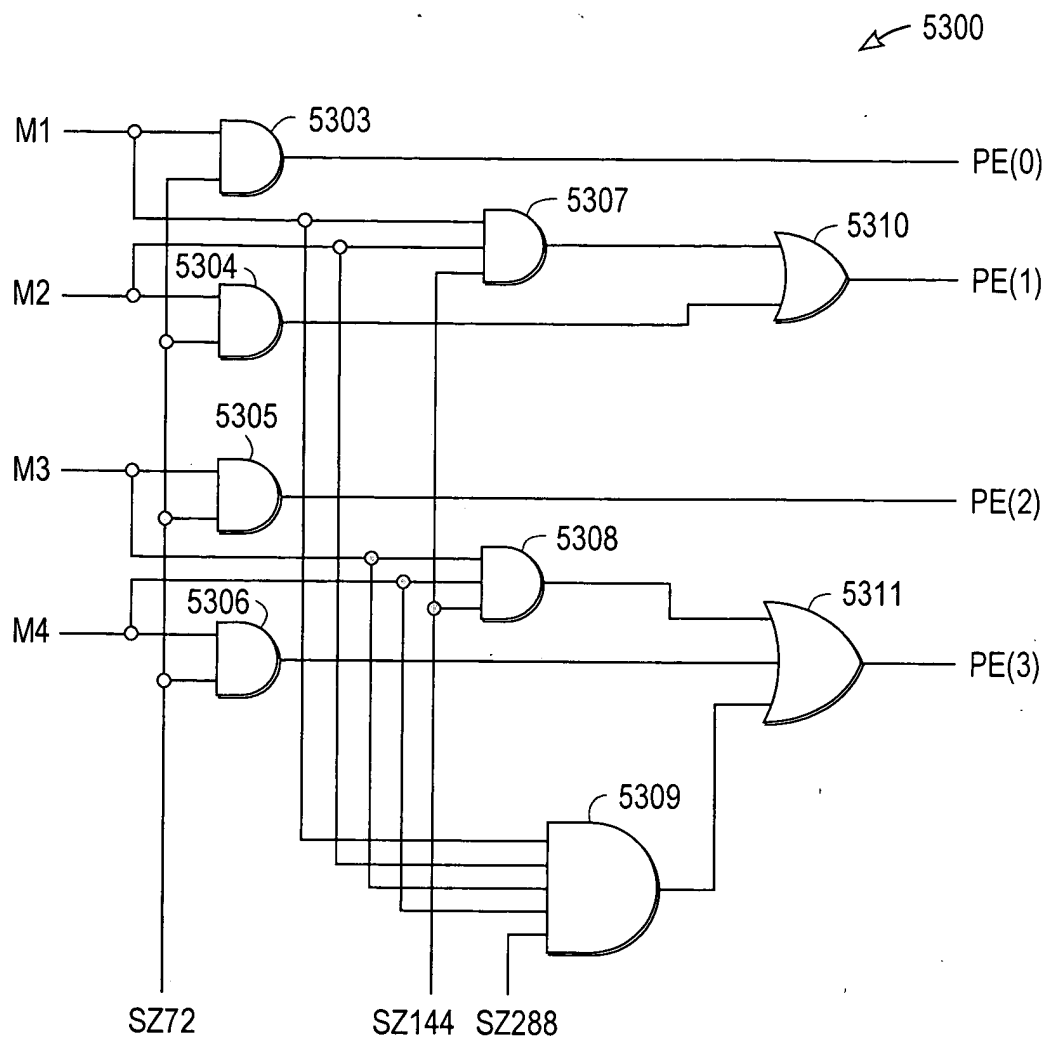


FIG. 55

Configuration	PE Inputs
$ZY \times W$	Set to M1-MZ for Corresponding Rows
$\frac{ZY}{2} \times 2W$	Set Every 2nd PE Input to the Corresponding First Group Match Results; Set All Other PE Inputs to Mismatch
$\frac{ZY}{4} \times 4W$	Set Every 4th PE Input to the Corresponding Second Group Match Results; Set All Other PE Inputs to Mismatch
• • •	• • •
$\frac{ZY}{(z-1)} \times (z-1)W$	Set Every (z-1) PE Input to the Corresponding (z-1) Group Match Results; Set All Other PE Inputs to Mismatch
$Y \times ZW$	Set Every Zth PE Input to the Corresponding Row Group Match Results; Set All Other PE Inputs to Mismatch

FIG. 56

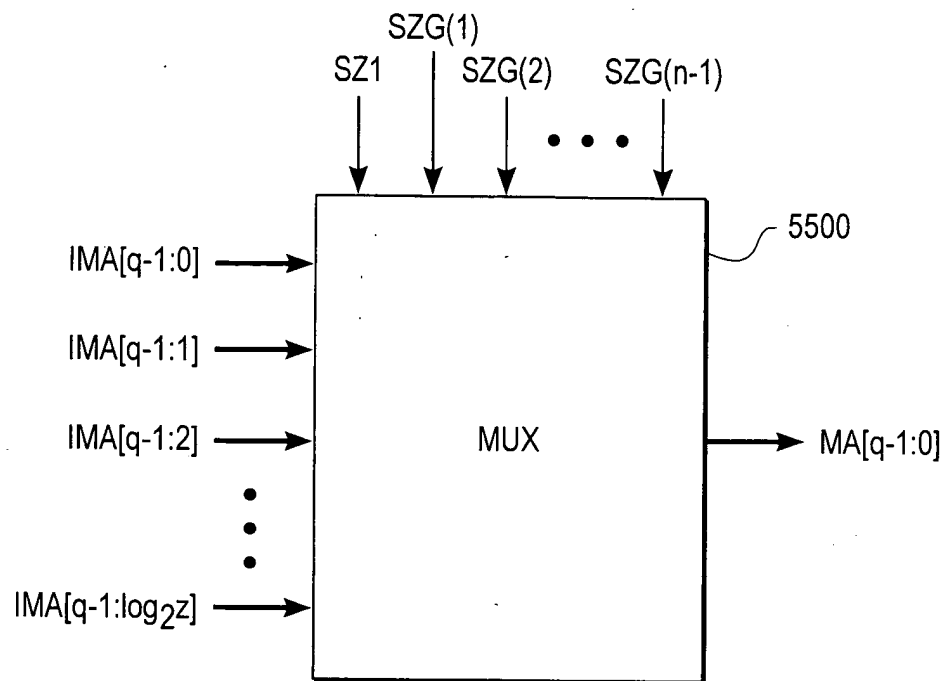


FIG. 57

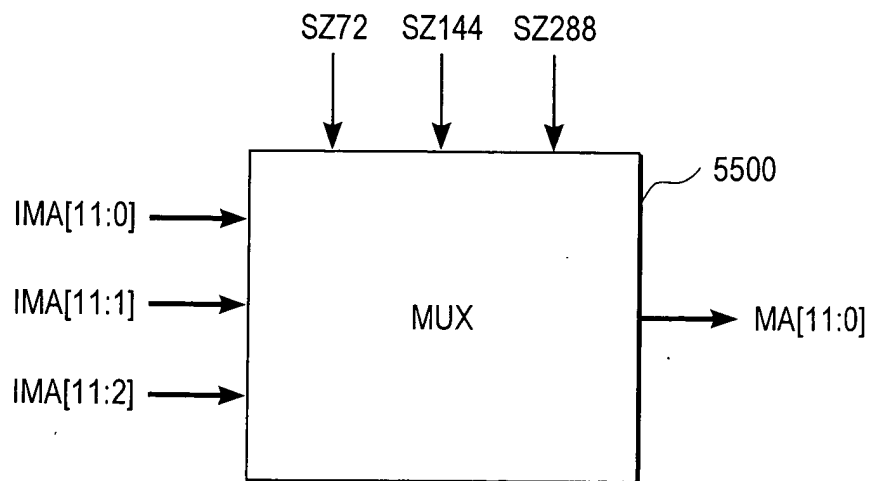


FIG. 58

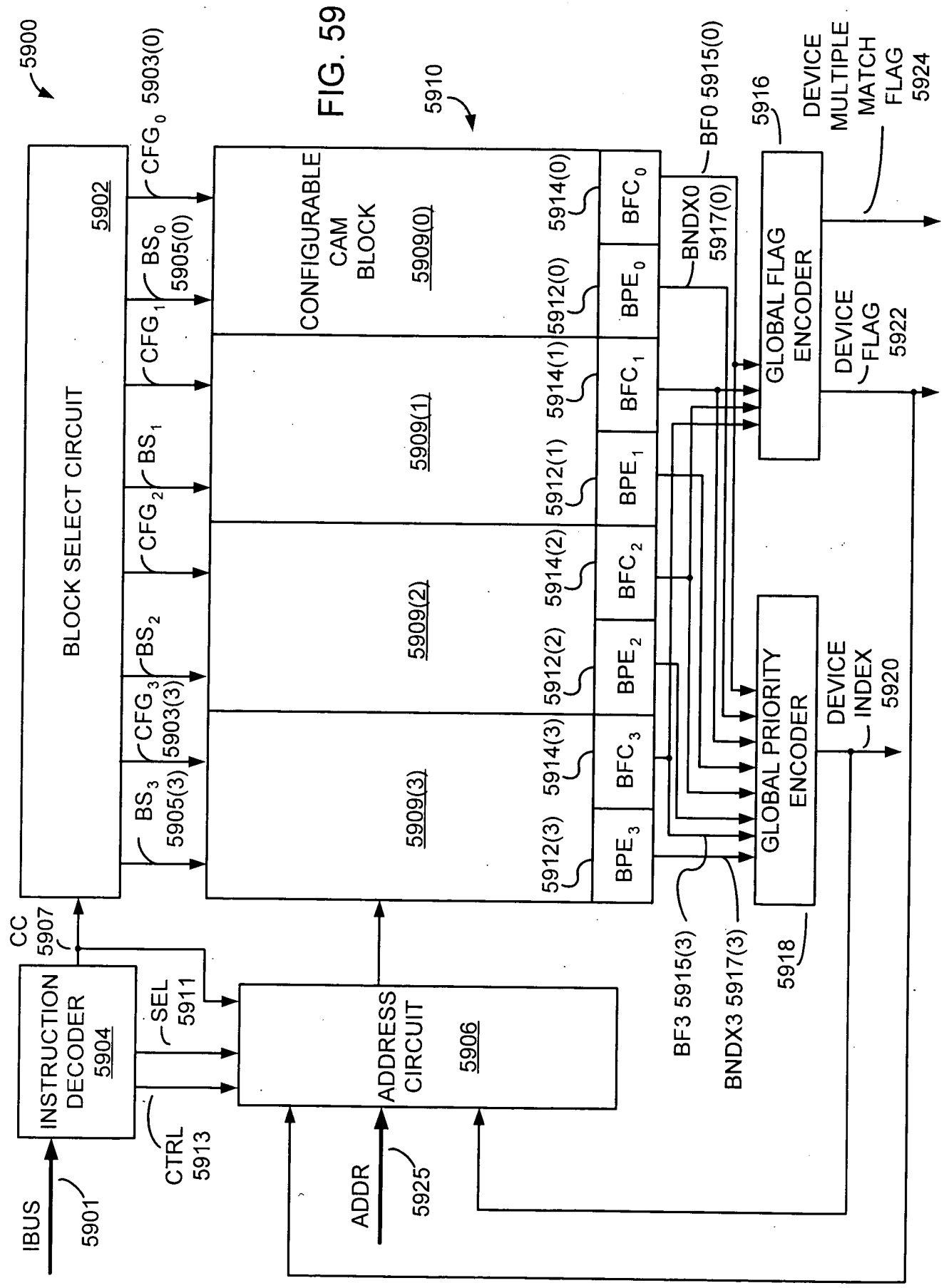


FIG. 59

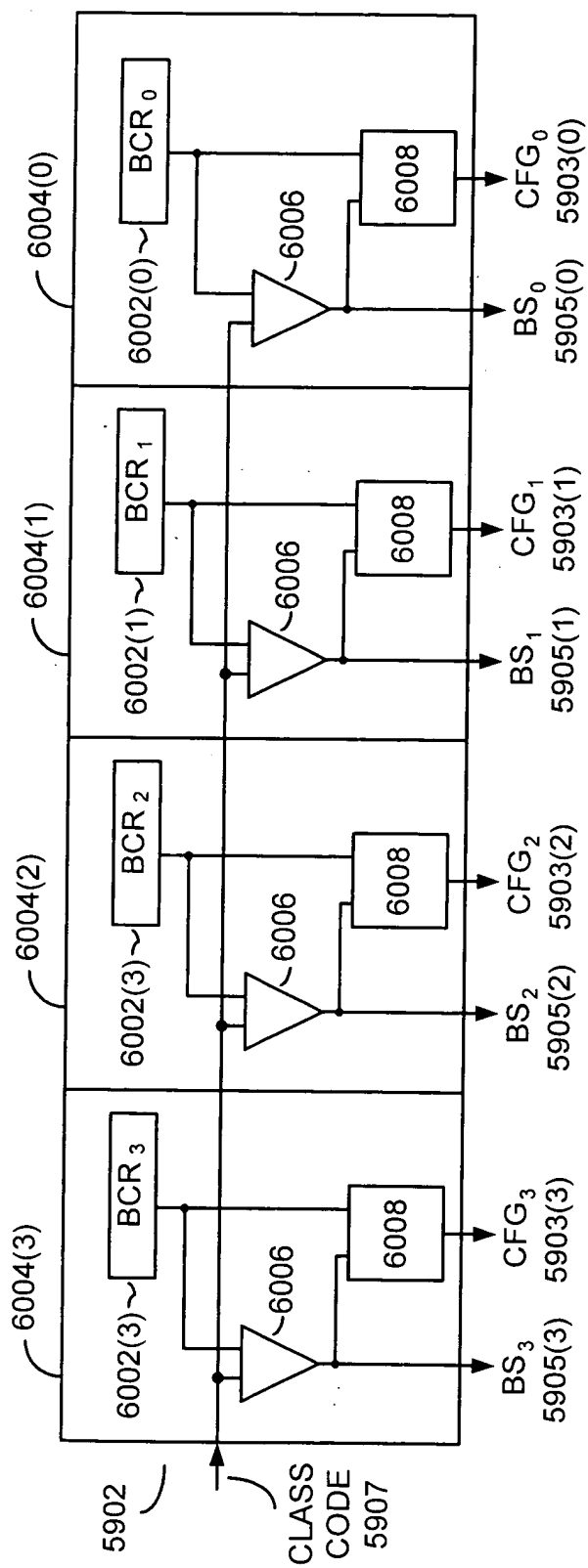


FIG. 60

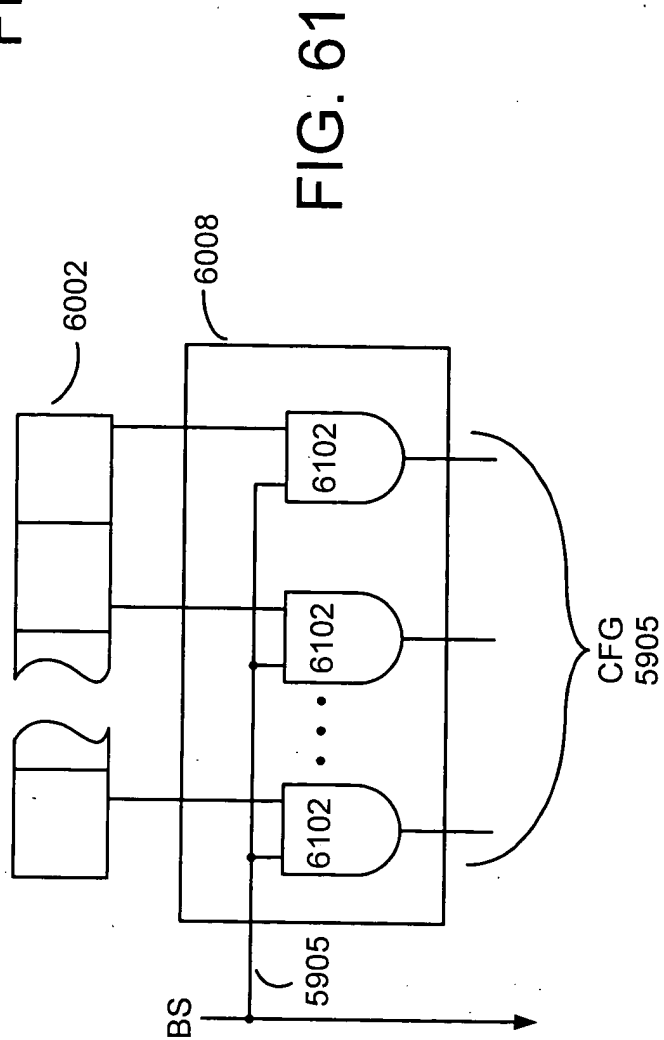


FIG. 61

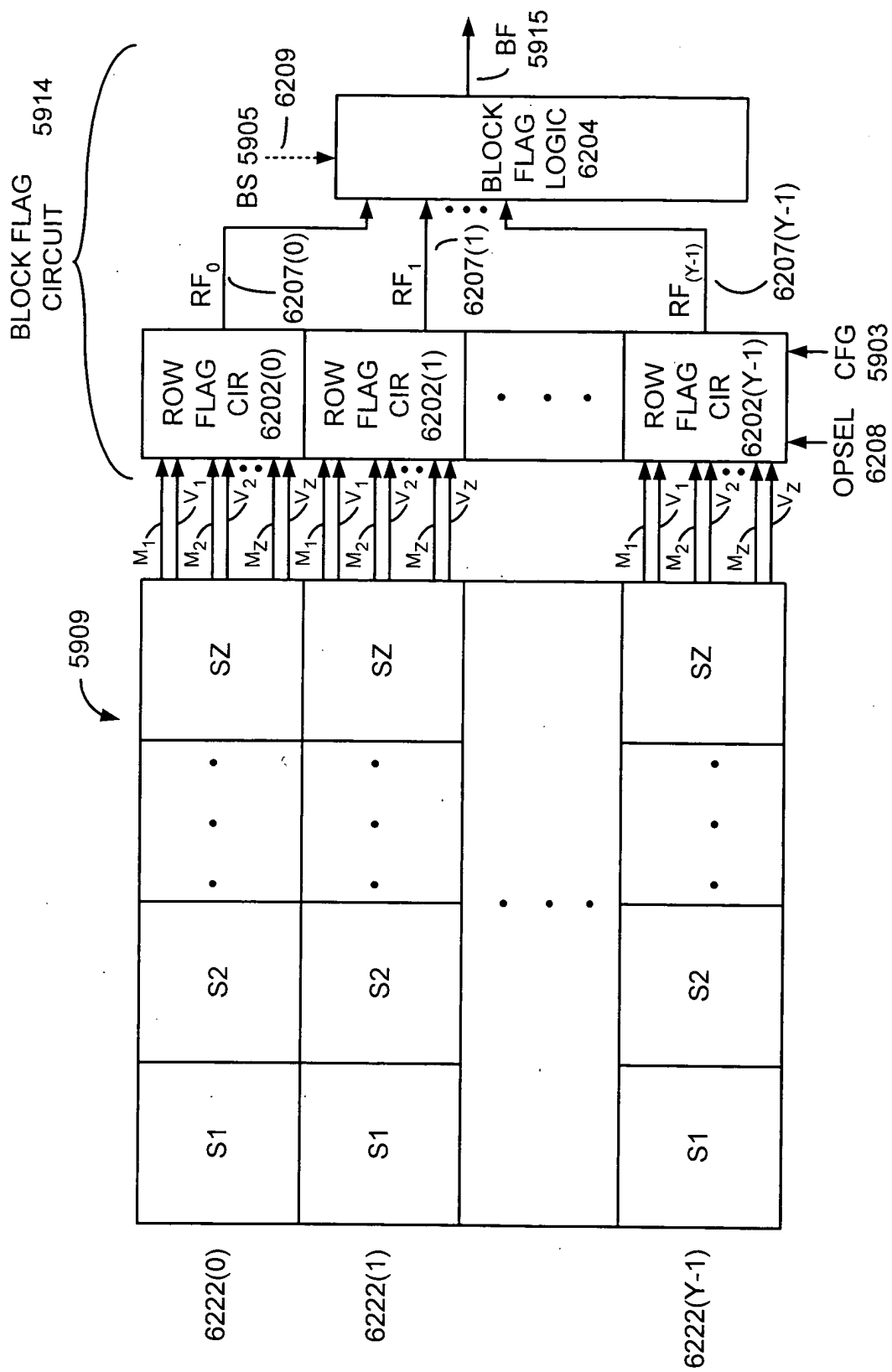


FIG. 62

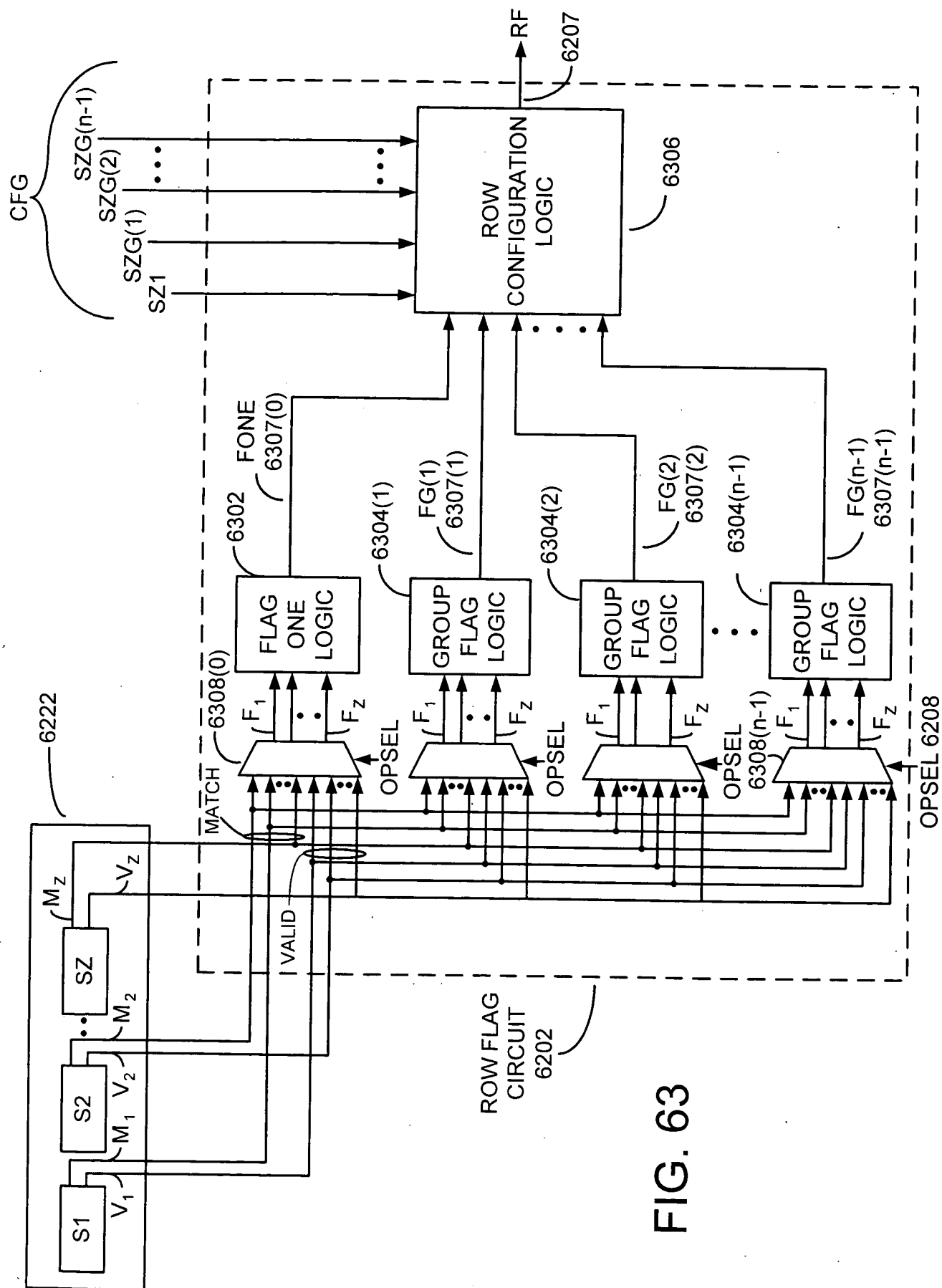


FIG. 63

FIG. 64

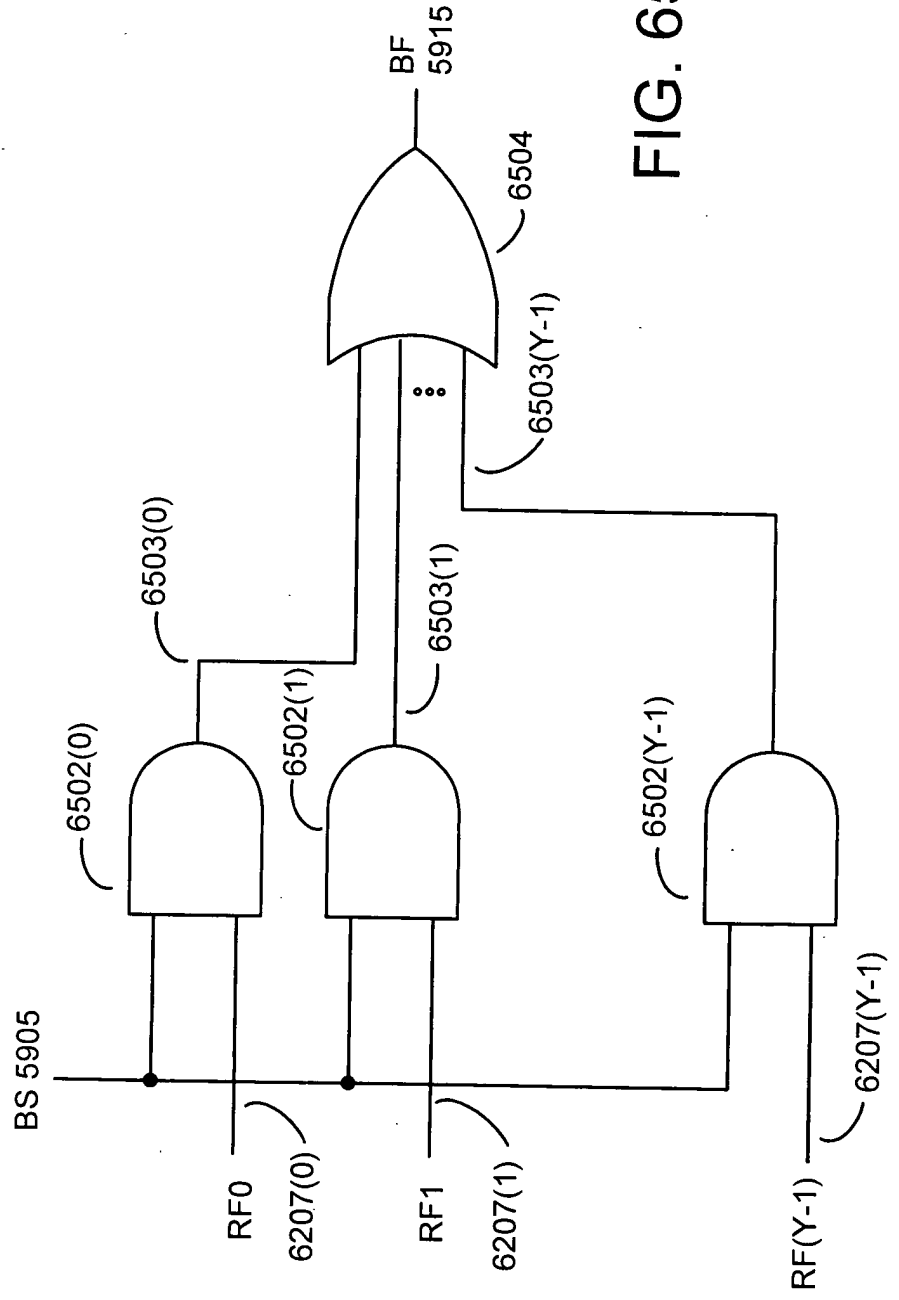
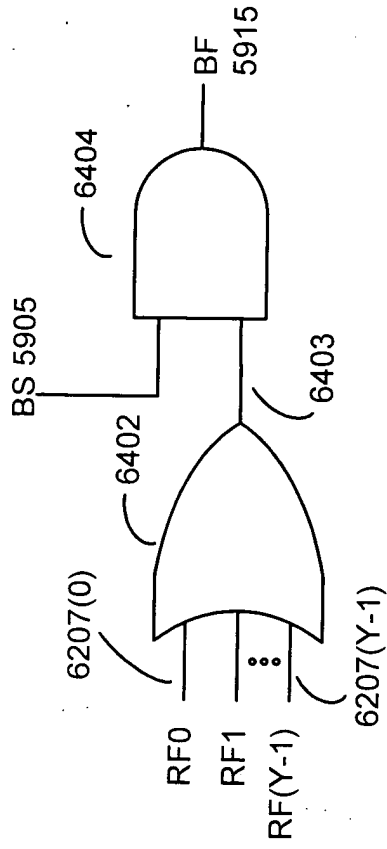


FIG. 65

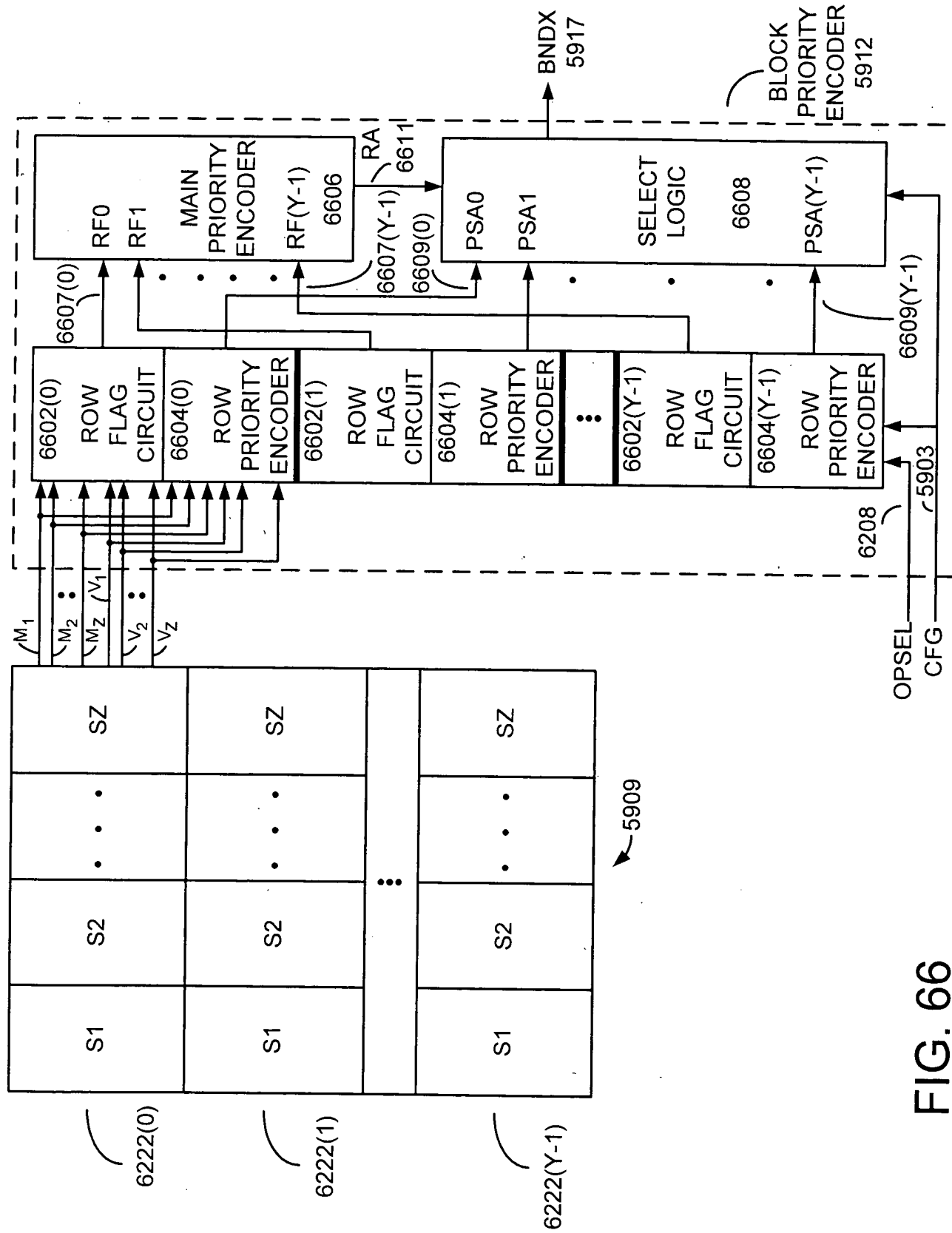


FIG. 66

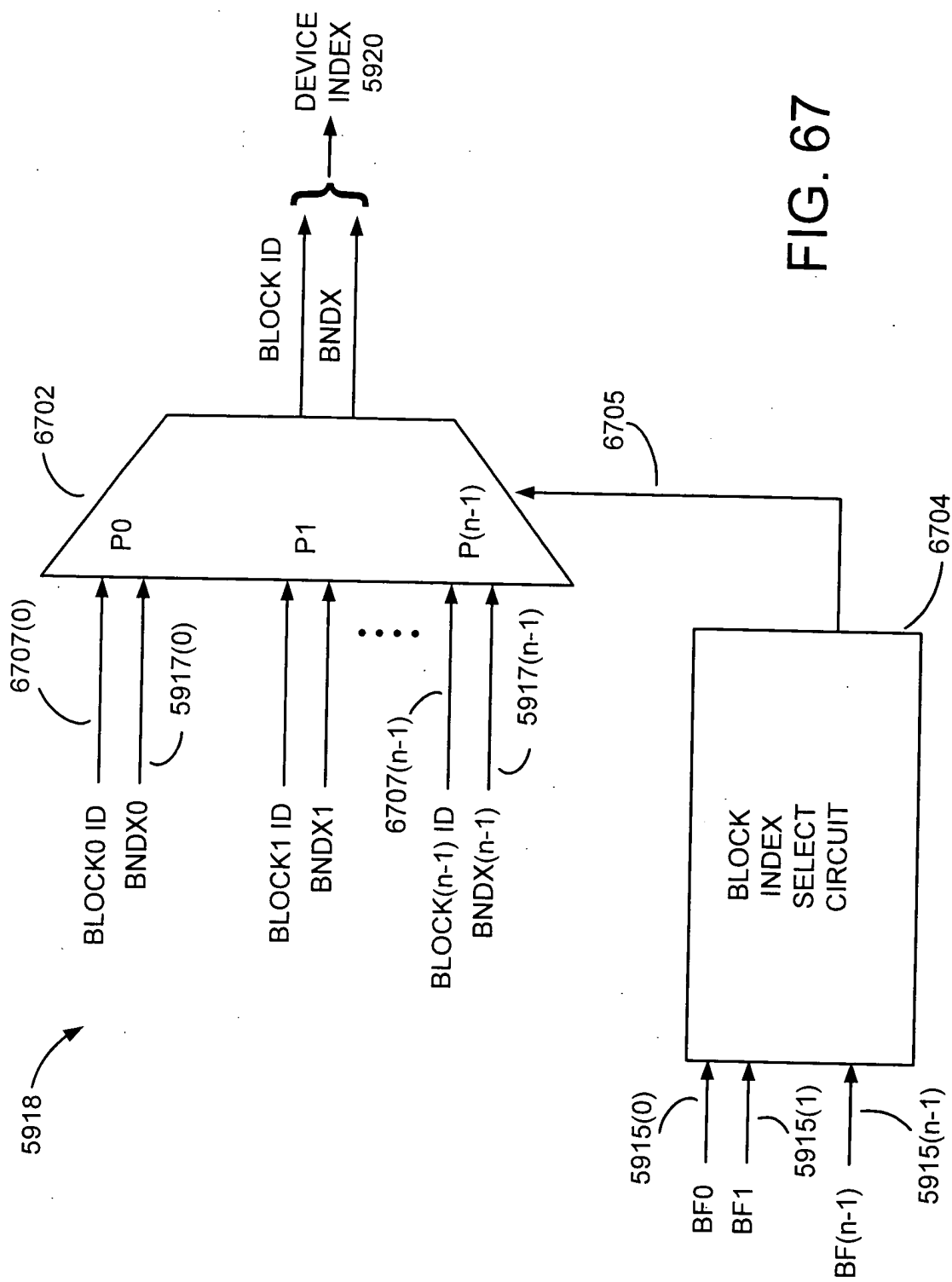


FIG. 67

FIG. 68

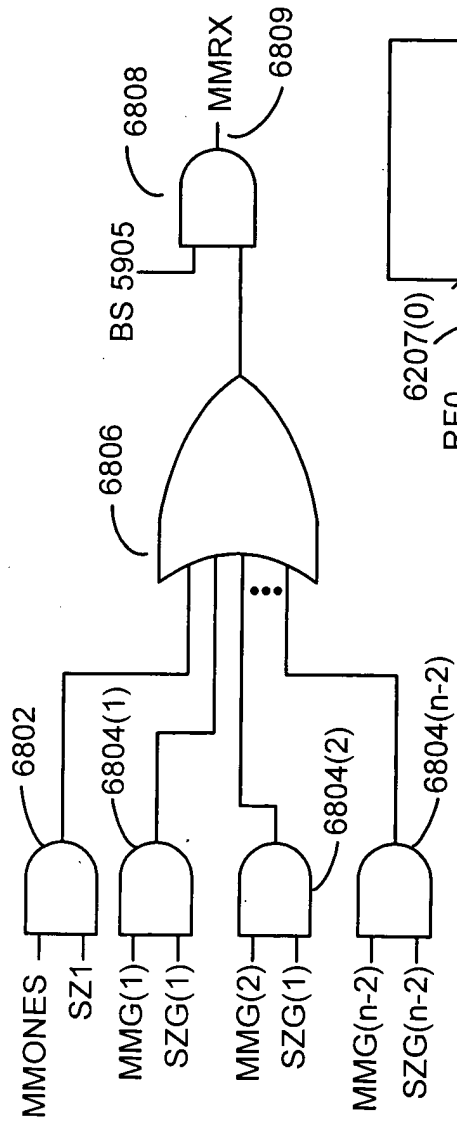


FIG. 69

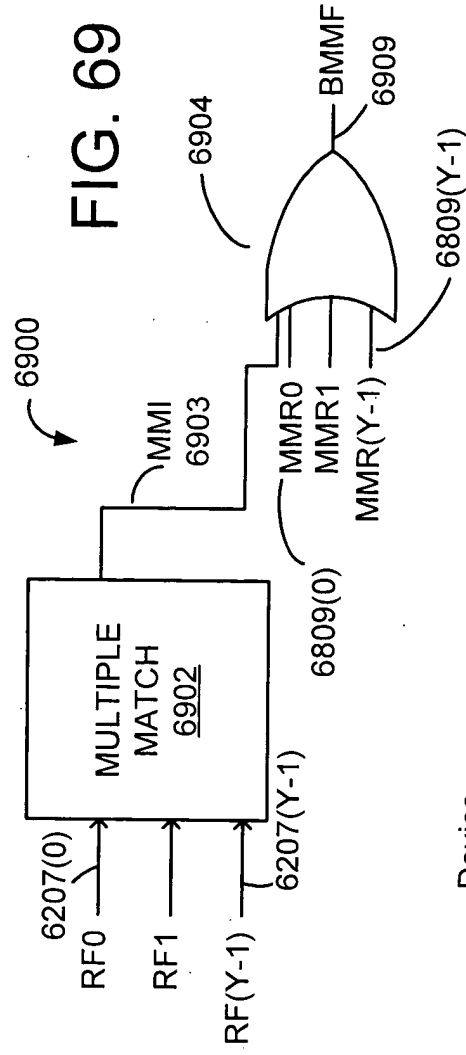
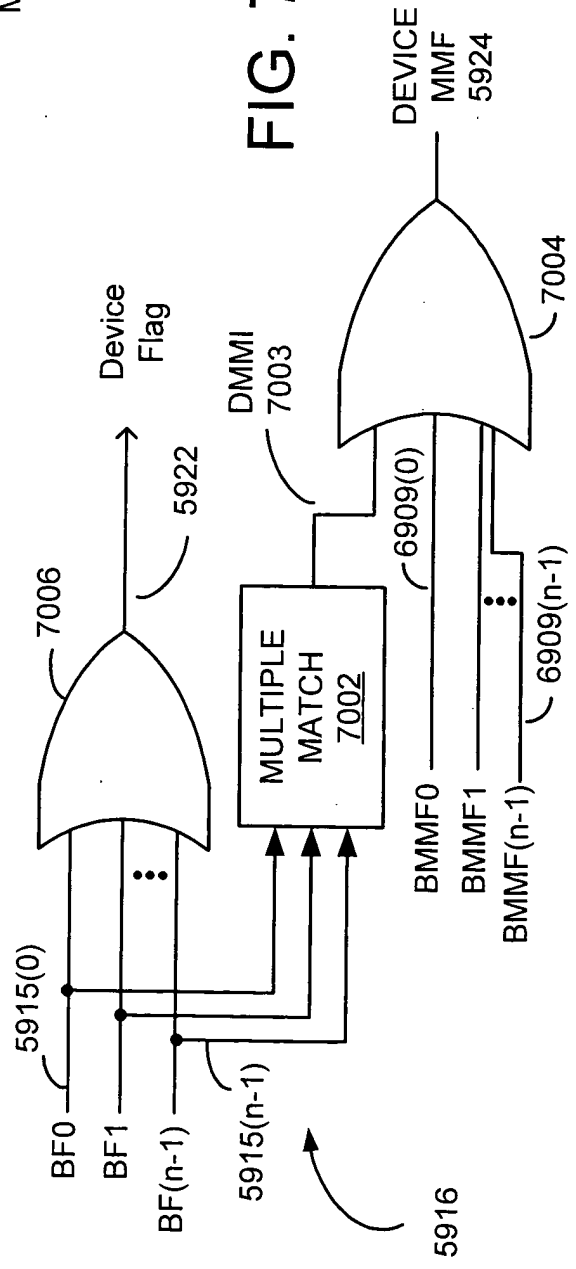


FIG. 70



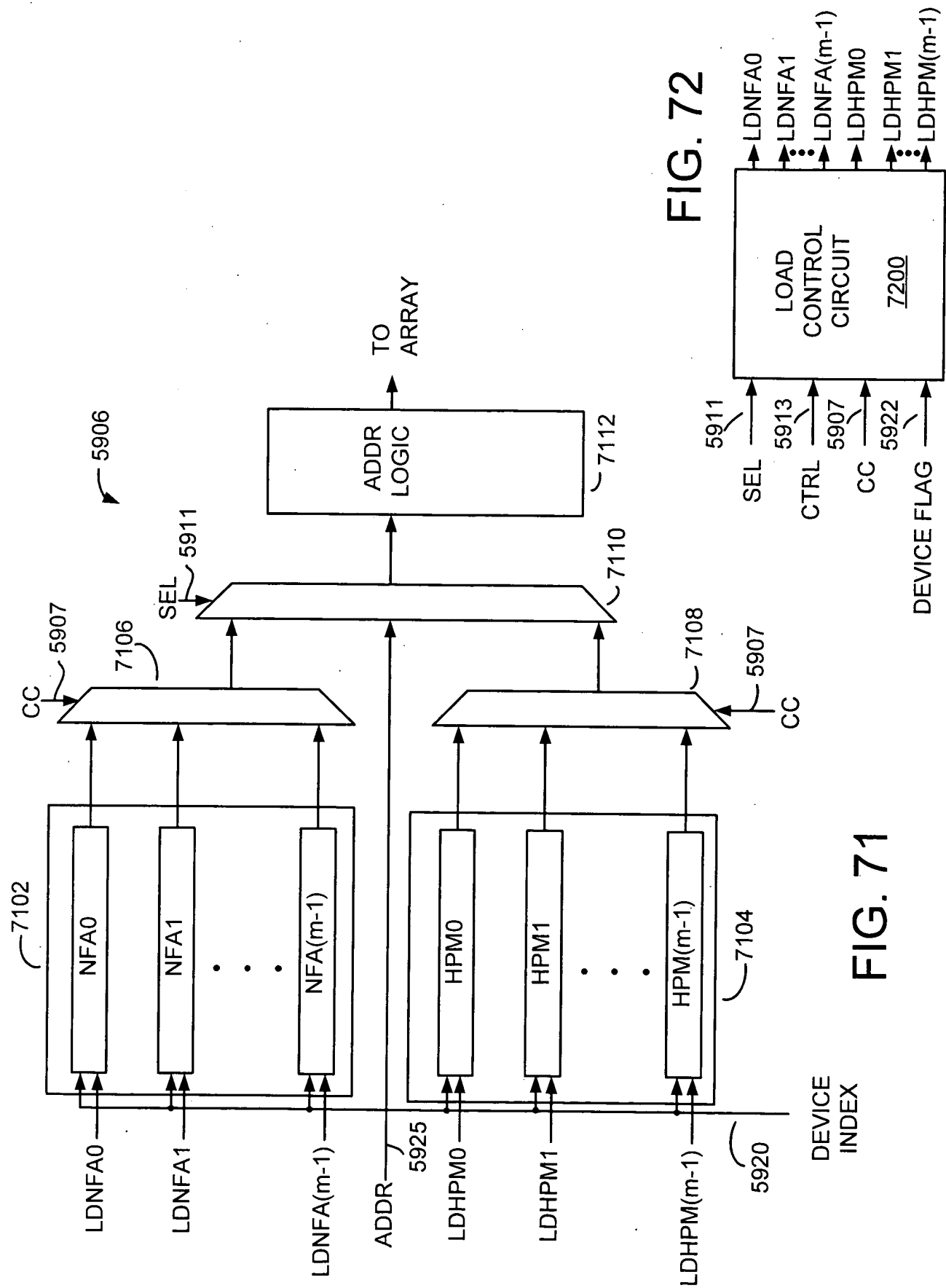


FIG. 72

FIG. 71

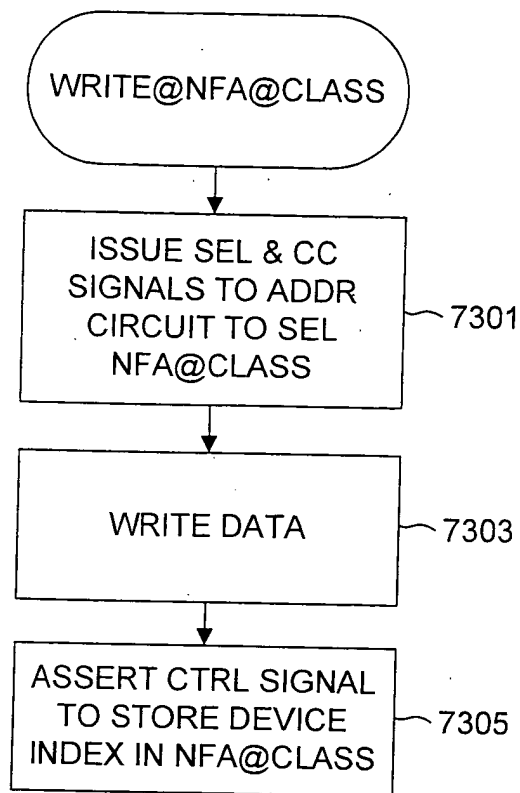


FIG. 73

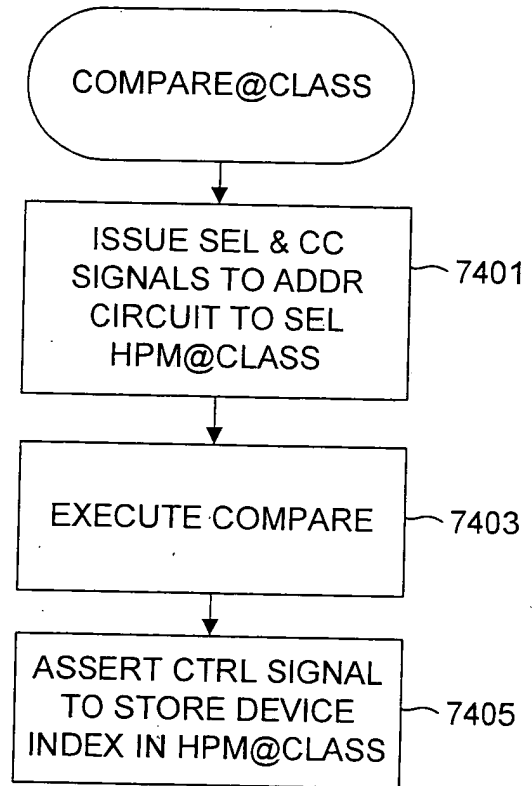


FIG. 74

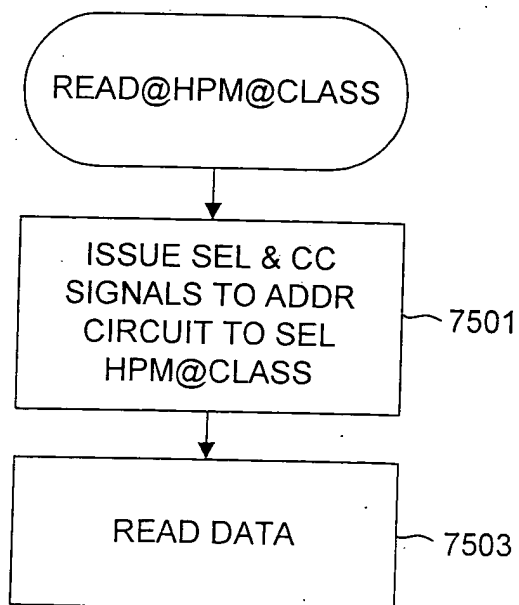


FIG. 75

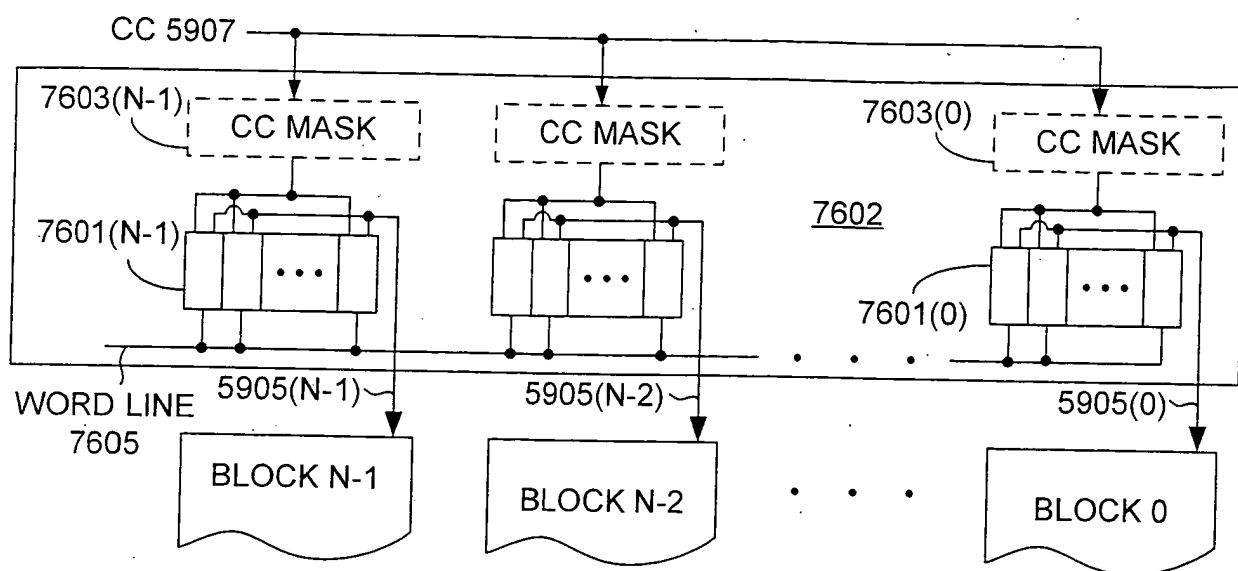


FIG. 76

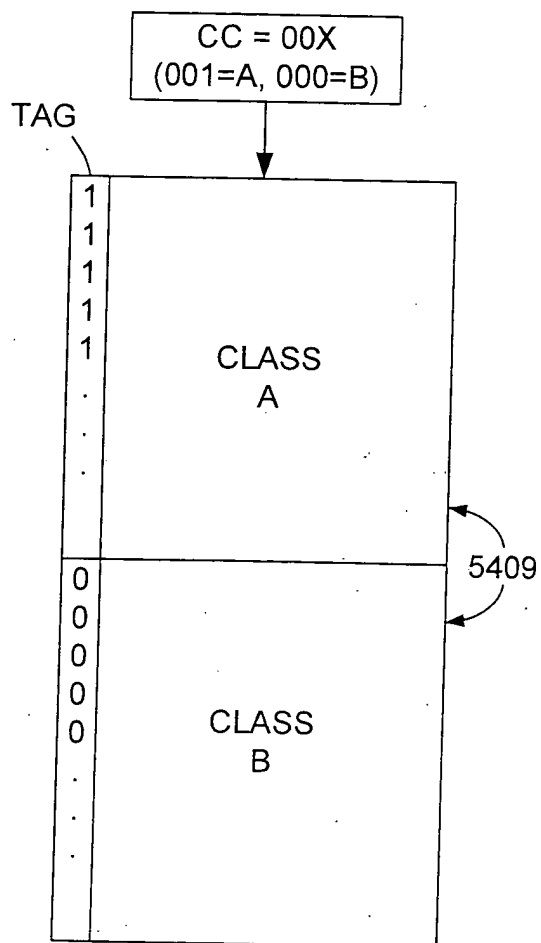


FIG. 77